TMEC
Thai Microelectronics Center

Wafer Fabrication
Part II

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Integrate Ideas Into Reality

Introduction to Wafer Fabrication

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- Introduction to TMEC
- History from Edison's Light Bulb to Pentium 4
- Semiconductor Materials
- Wafer Preparation
- Wafer Fabrication Processes
- Thin Film Deposition Process
- Patterning Process
- Etching Process
- Doping Process
- Contamination

Microelectronics Fabrication

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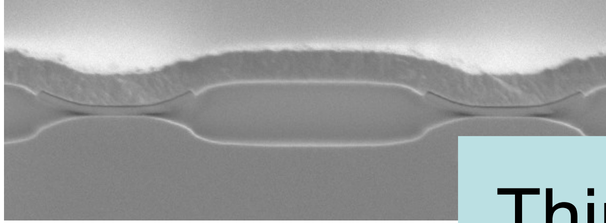
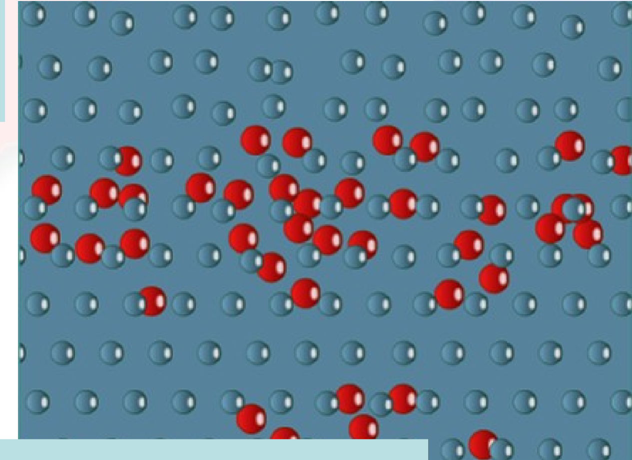
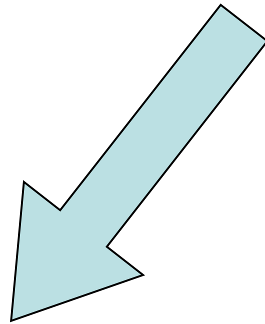
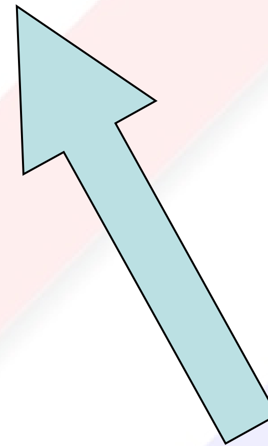


Thin Film Deposition

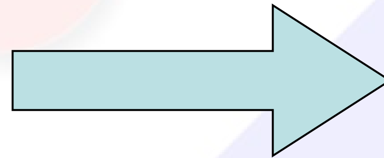




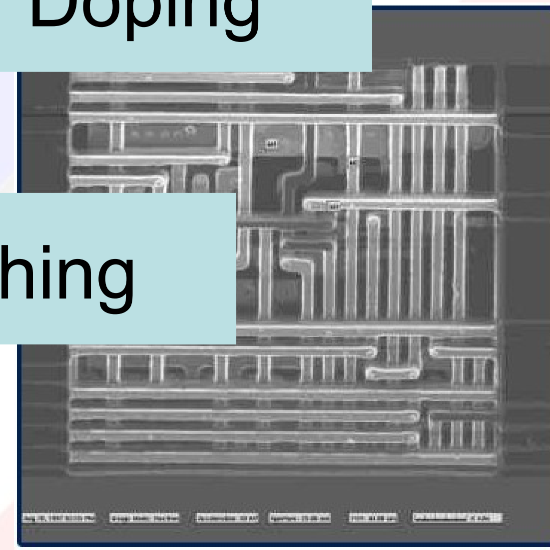


Doping

Lithography



Etching



Wafer Fabrication Processes

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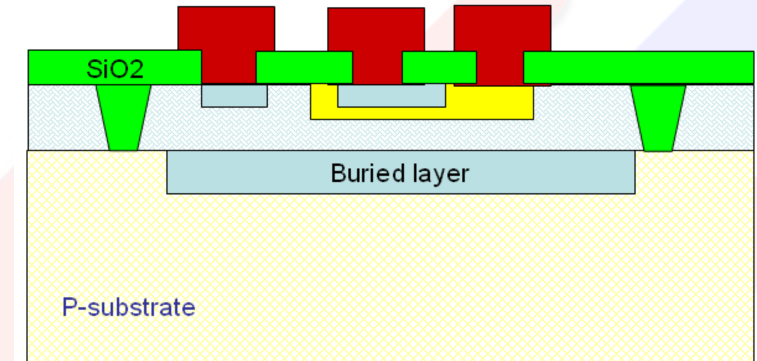
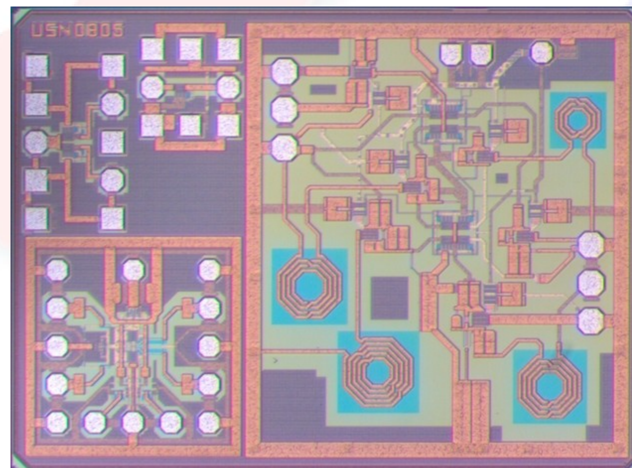
CMOS Process



Bipolar Process



BiCMOS Process

Technologie 0.25µm BiCMOS SiGe,Philips

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p-type Silicon Substrate

1. Starting wafer
2. n-well
3. Active
4. Gate
5. Junction
6. ILD
7. Contacts and metal 1
8. Vias and metal 2
9. Passivation

Wafer

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p-type Cz wafer

p-type

Process flow

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p-type Silicon Substrate

1. Starting wafer
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4. Gate
5. Junction
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7. Contacts and metal 1
8. Vias and metal 2
9. Passivation

n-well

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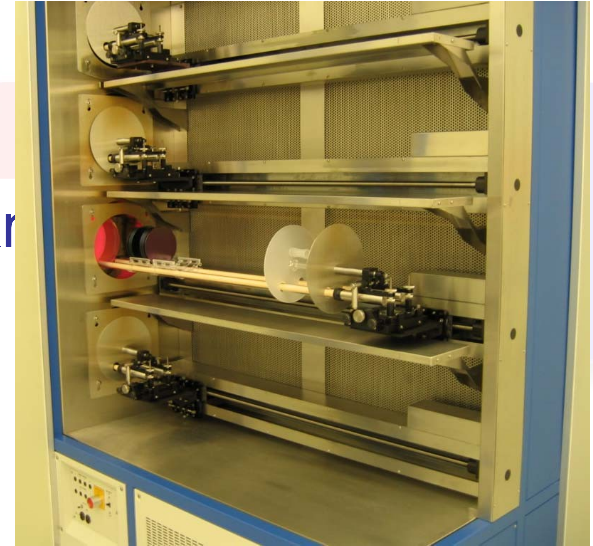
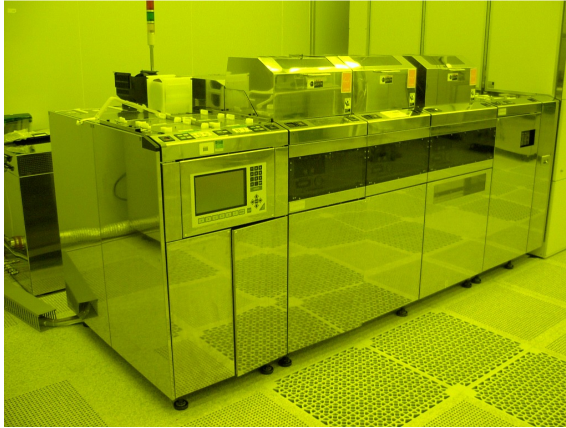


Initial oxidation: O /H (Thickr
420 nm)

n-well



Photolithography : NWELL

Photoresist (PR)

p-type

n-well

Dry etch oxide

n-well

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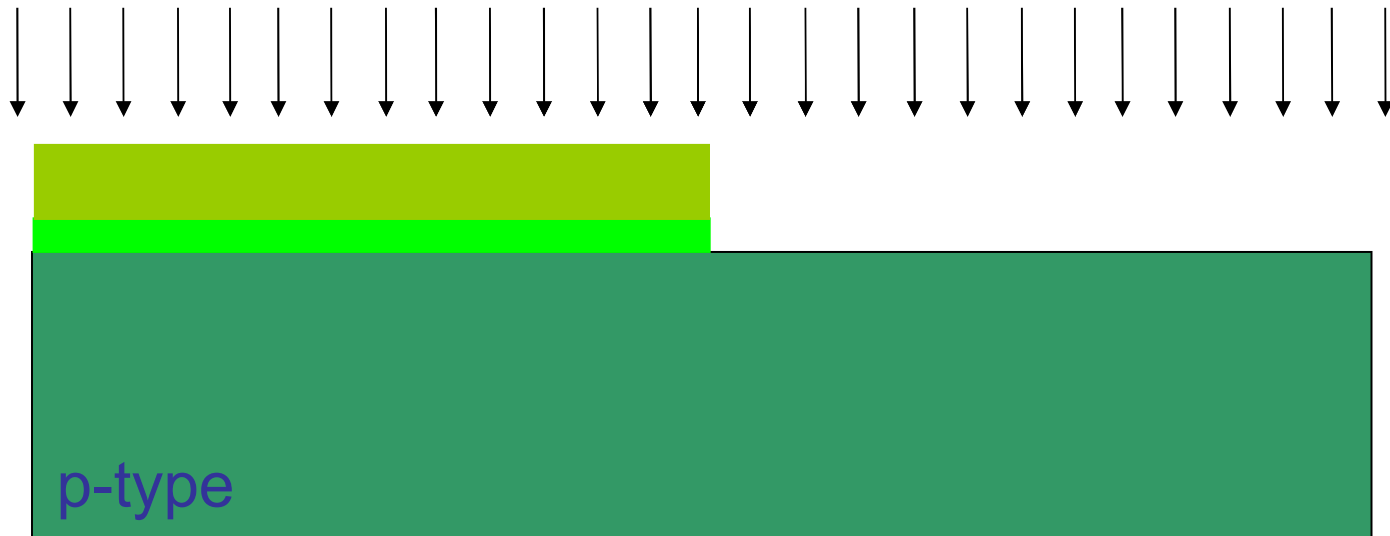
n-well implantation : Phosphorus
(3x10 cm , 100 keV)



n-well

Resist strip

n-well

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n-well drive : Anneal : N_2
Differential Oxidation : O_2/H_2
Anneal : N_2

Process flow

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p-type Silicon Substrate

1. Starting wafer
2. n-well
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7. Contacts and metal 1
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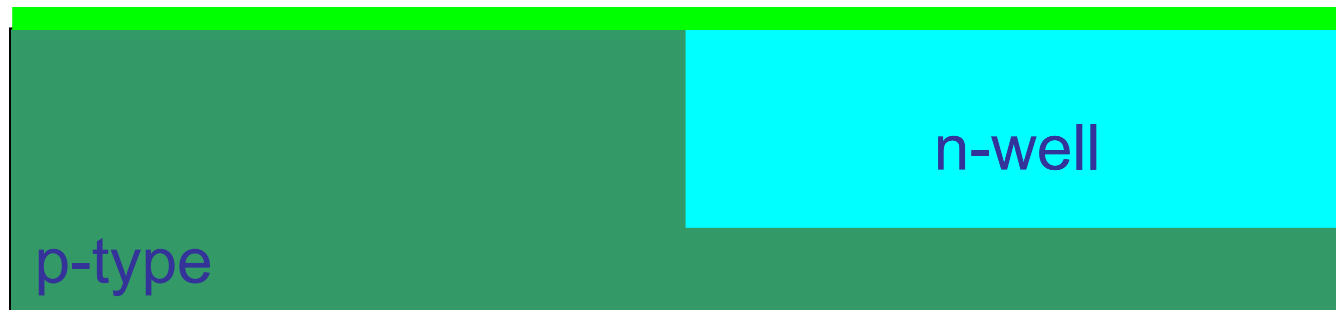
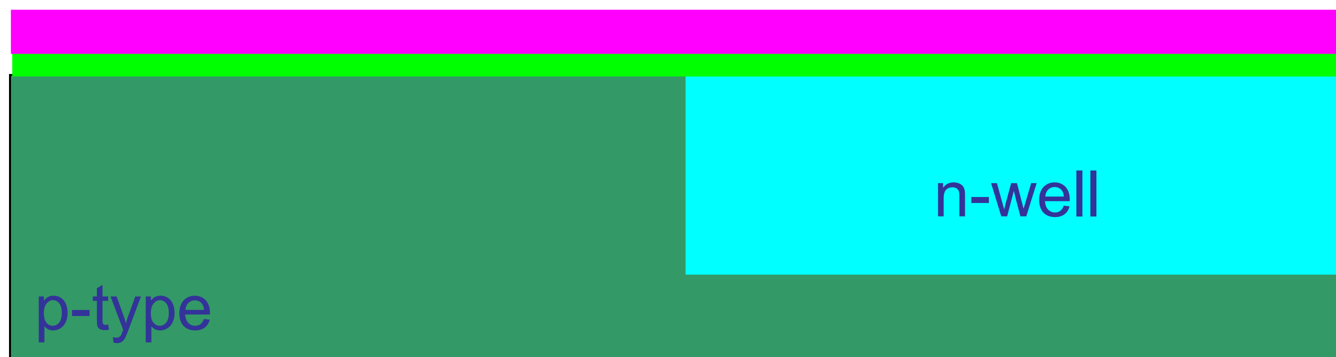
Active

Wet etch all oxide + Pad oxidation (20 nm)

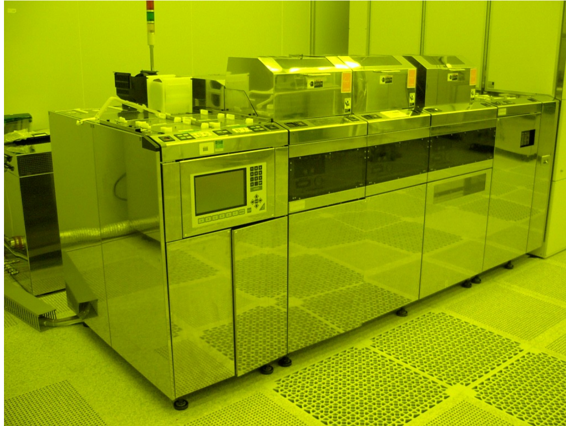


Active

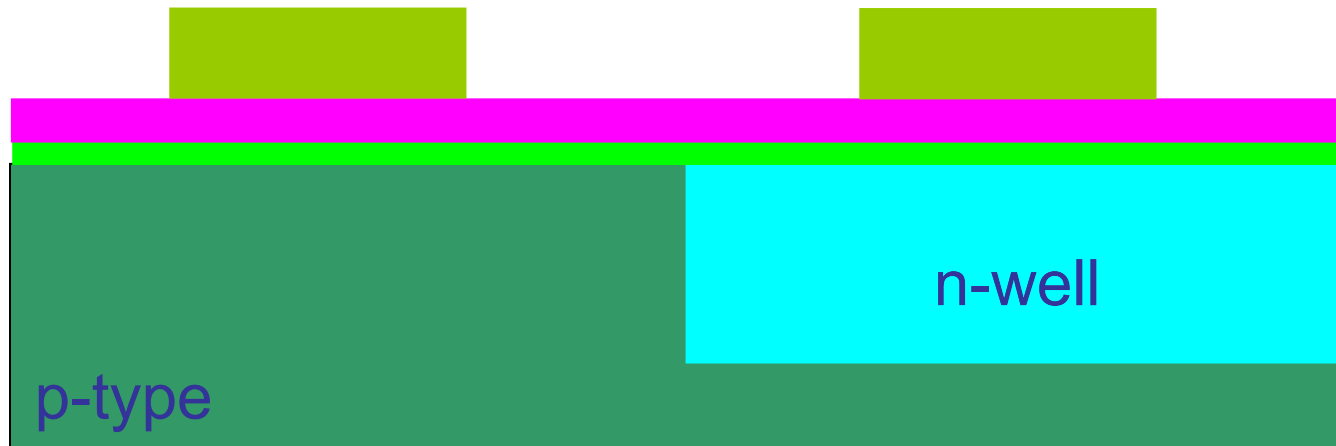
Deposition : Nitride (150 nm)



Active

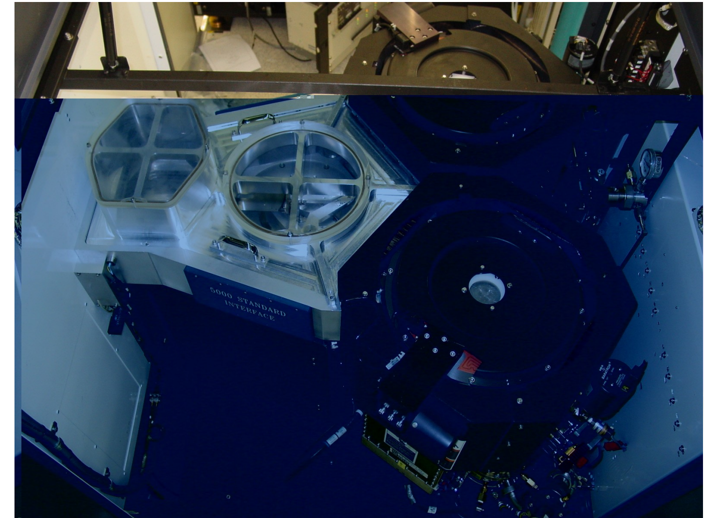


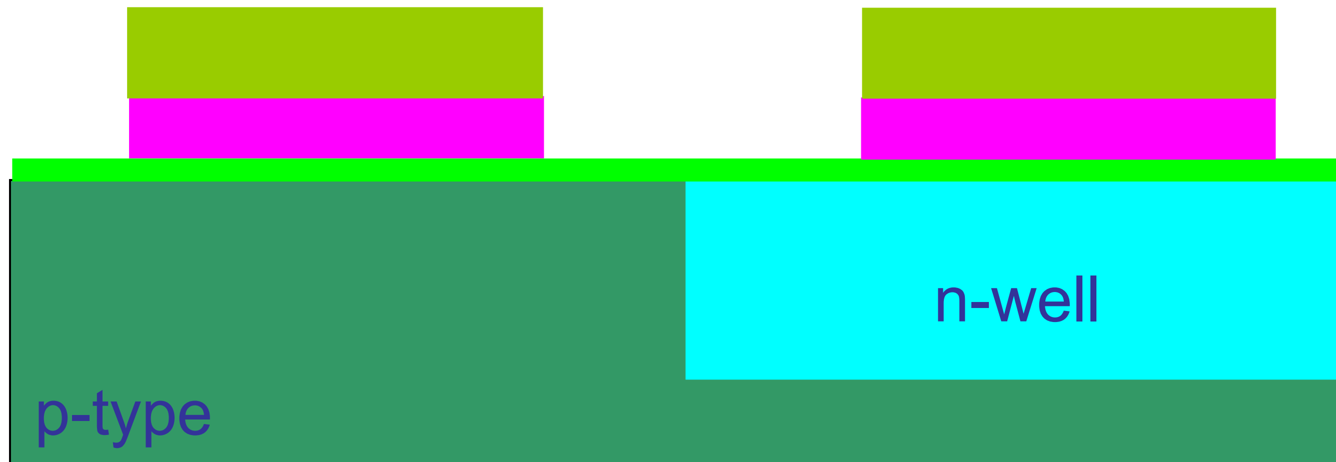
Photolithography : ACTIVE



Active

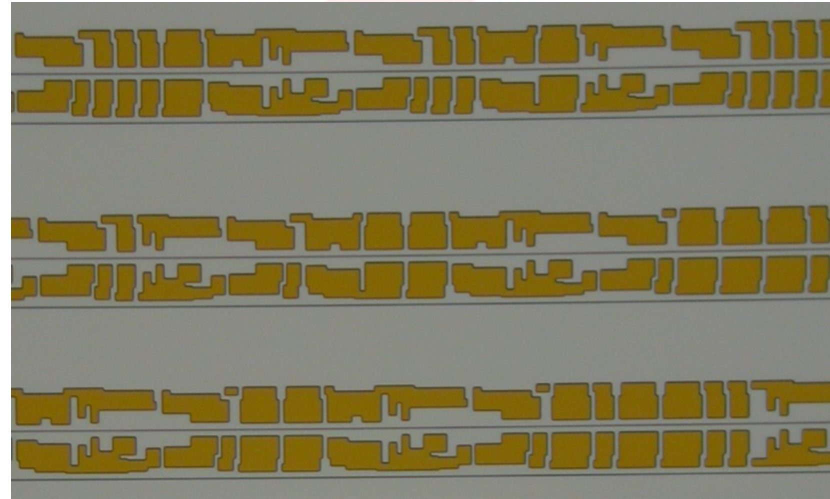
Dry etch nitride

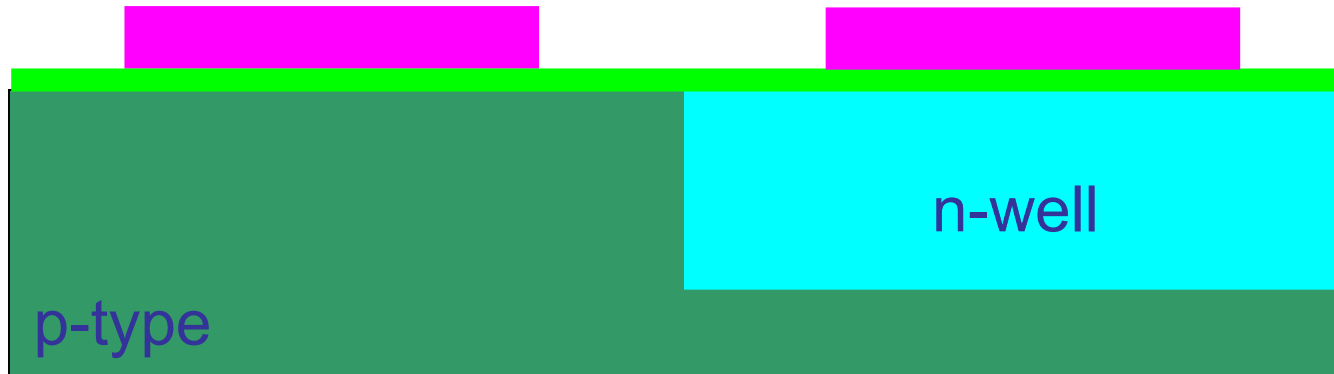




Active

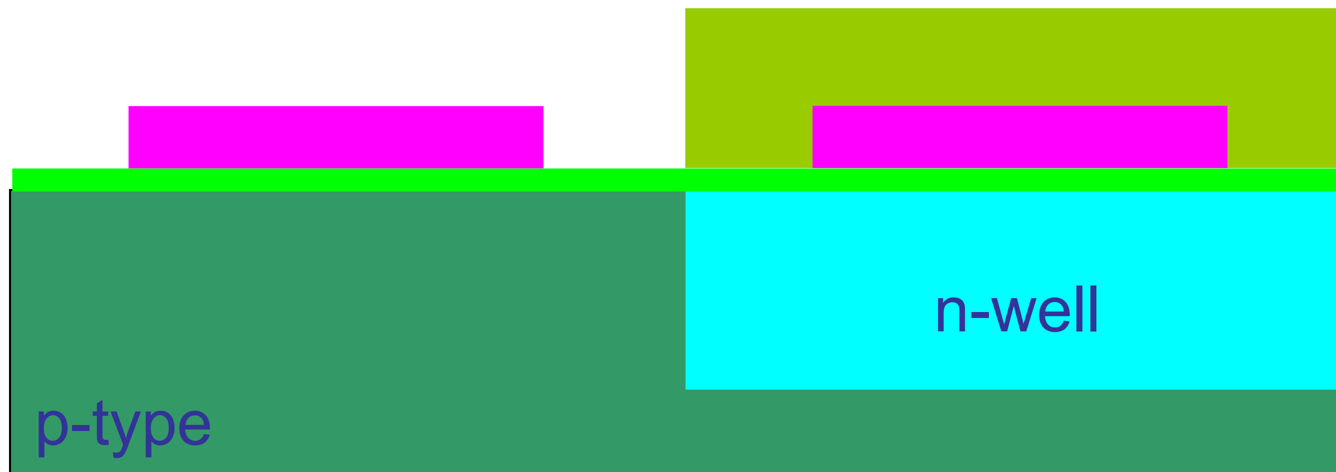
Resist strip





Active

Photolithography : NFIELD



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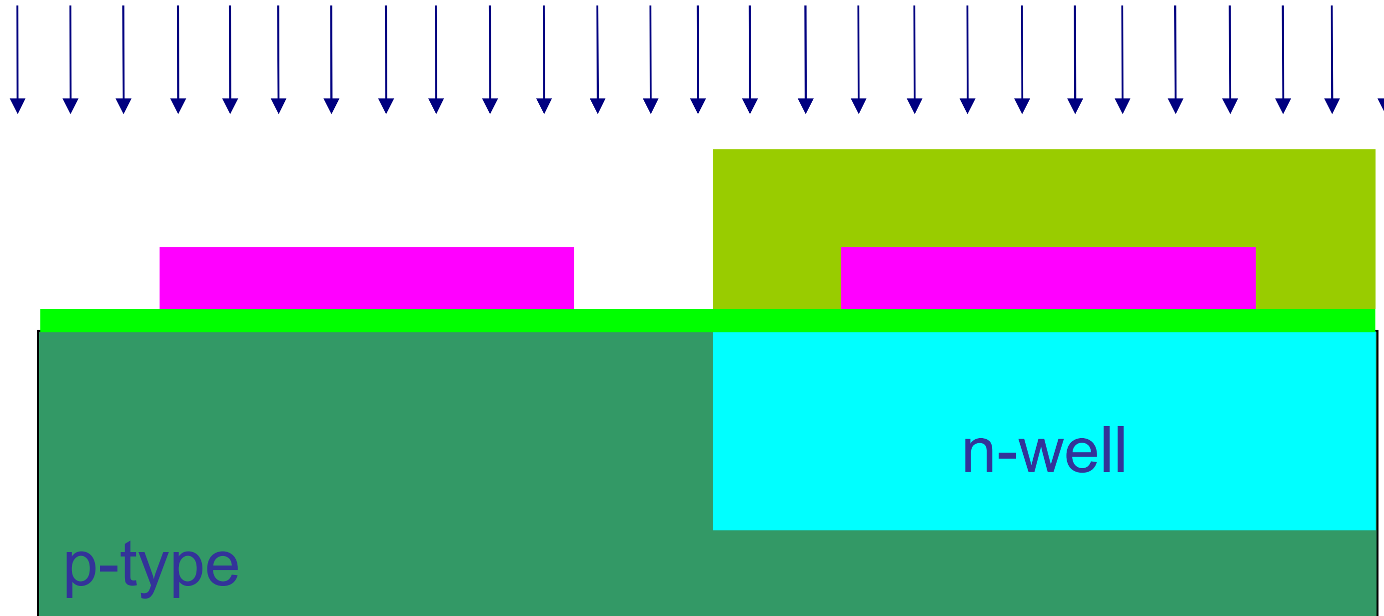
NField implantation : Boron (8x10 cm , 60 keV)



Active

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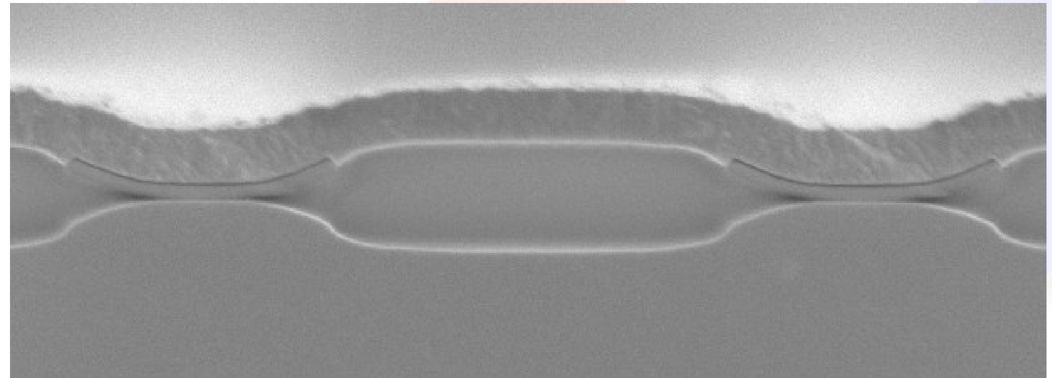
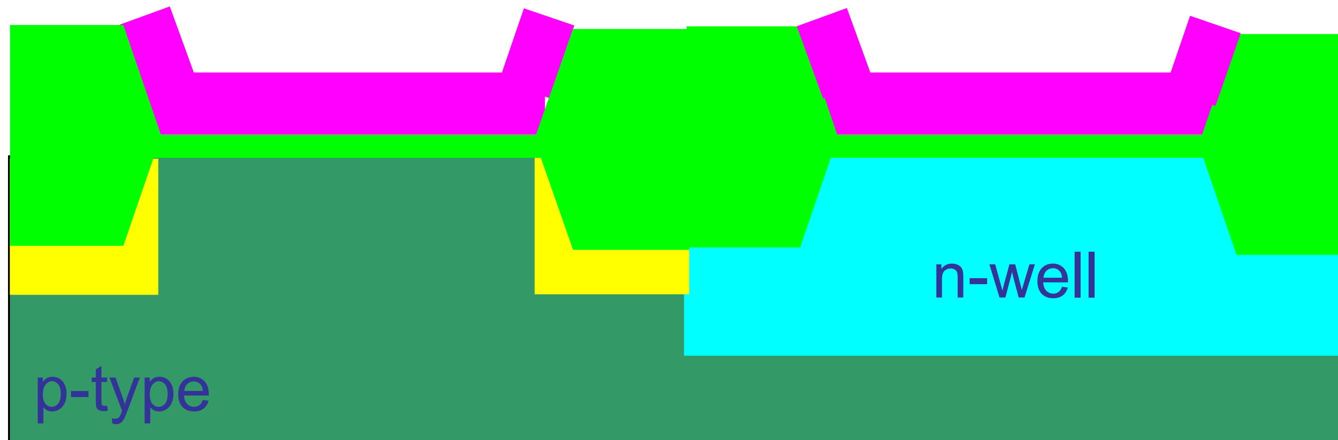
Resist strip

Active

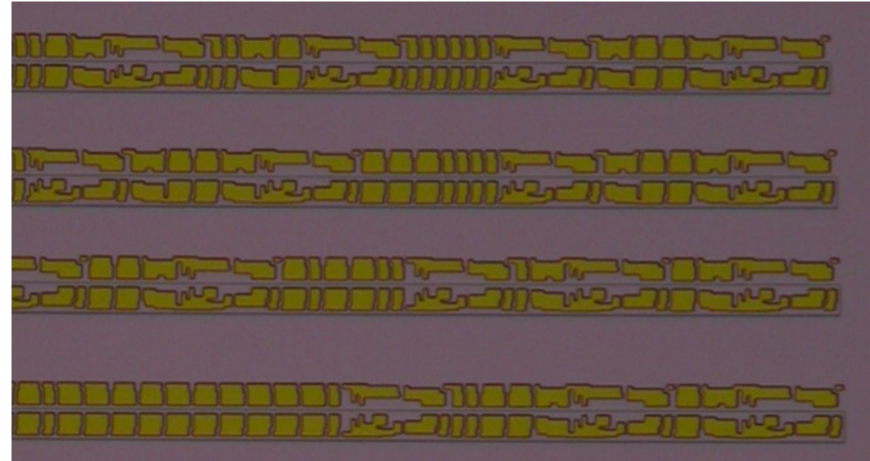
Field oxidation : O /H

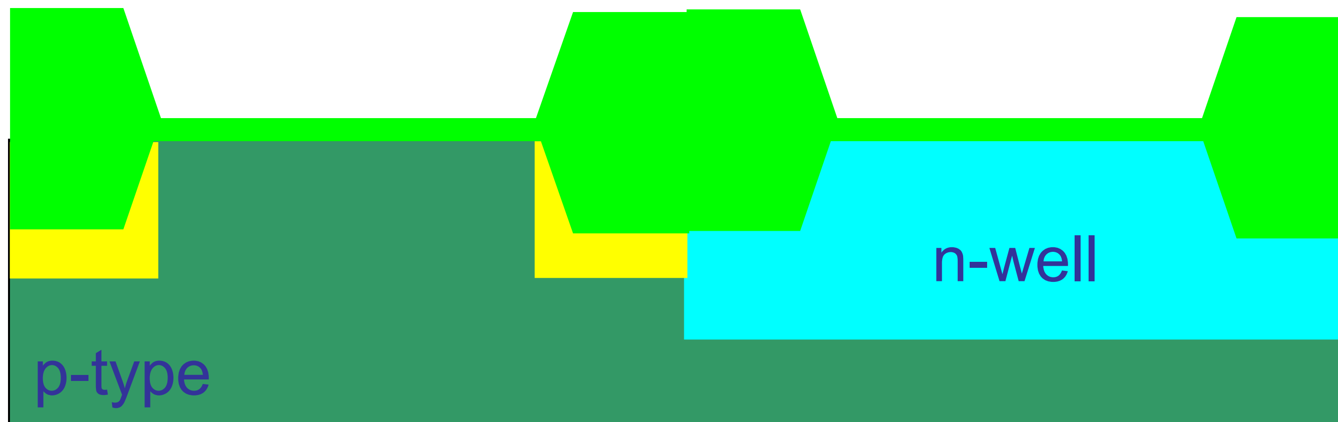




Active

Wet etch Nitride





Process flow

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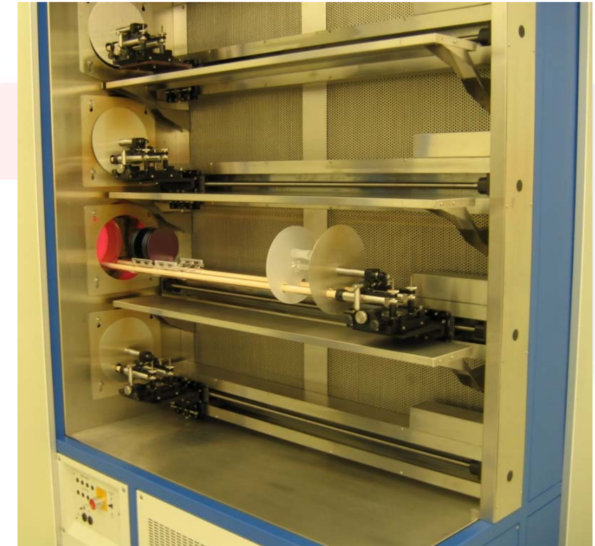
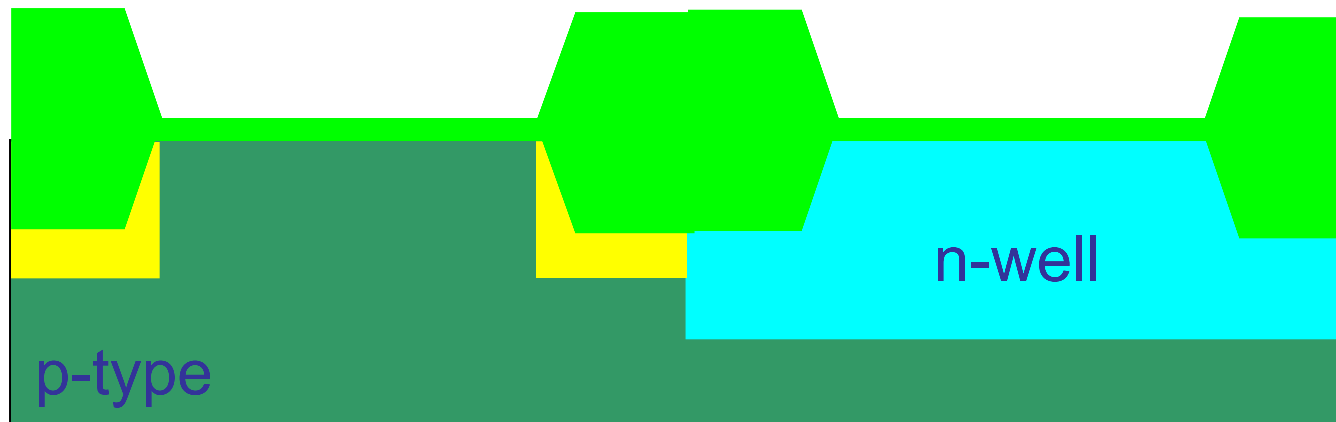
p-type Silicon Substrate

1. Starting wafer
2. n-well
3. Active
4. Gate
5. Junction
6. ILD
7. Contacts and metal 1
8. Vias and metal 2
9. Passivation

Gate

Etch Pad oxide + WR
oxidation : H /O (50 nm)





Gate

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Photolithography : NFIELD

Gate

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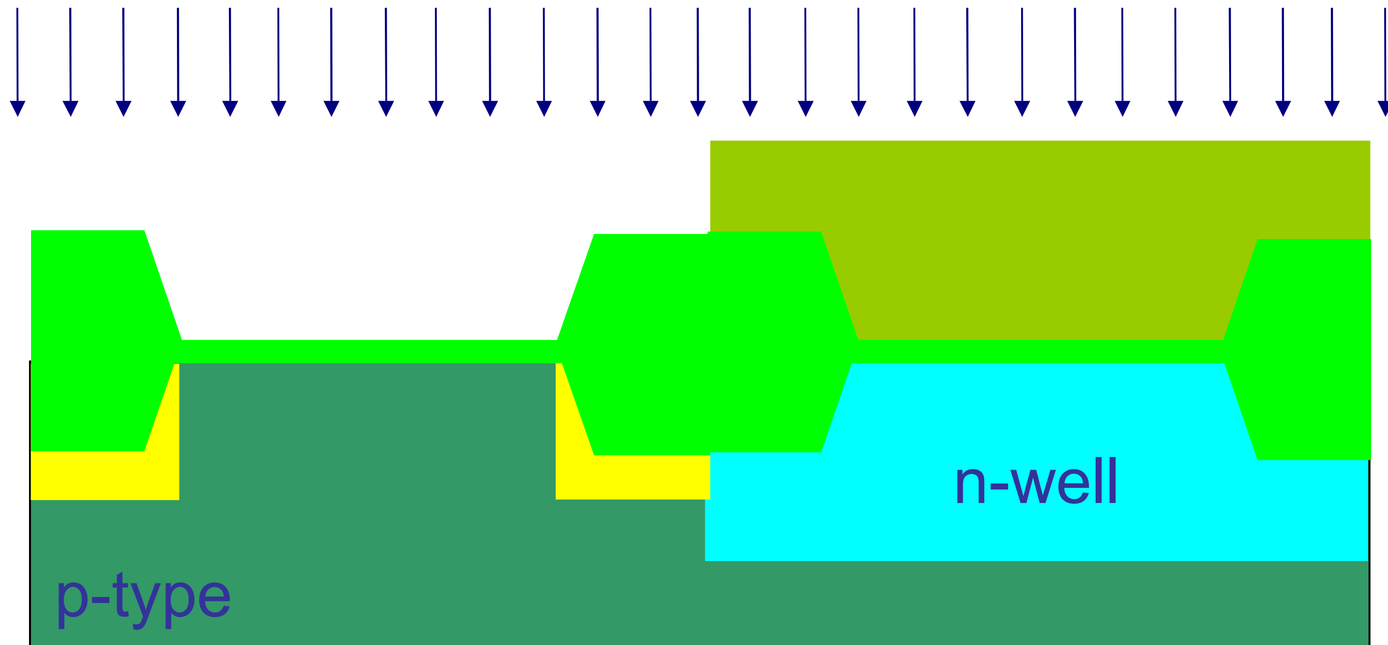
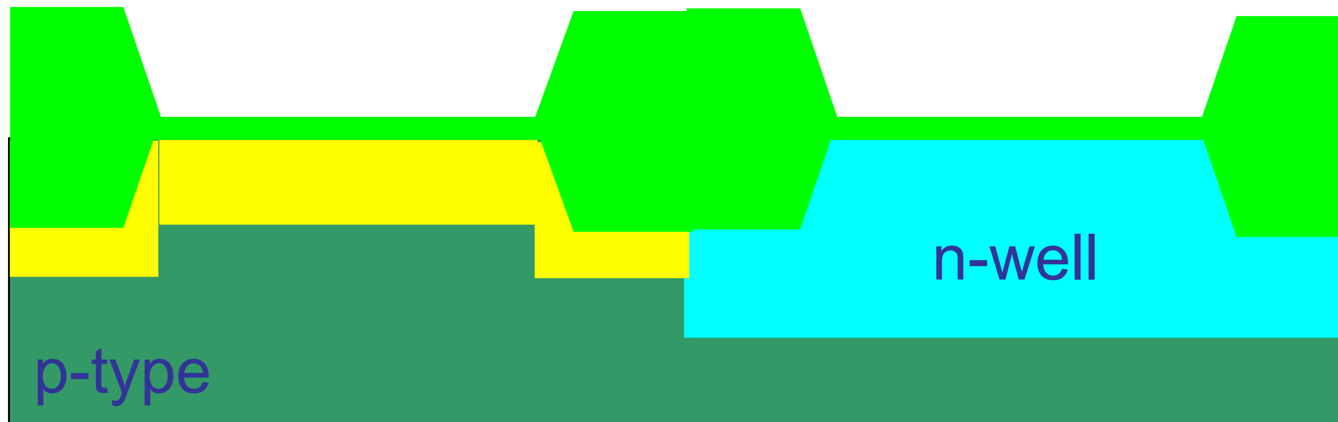
APT Implantation : Boron
(6.5x10 cm , 110 keV)



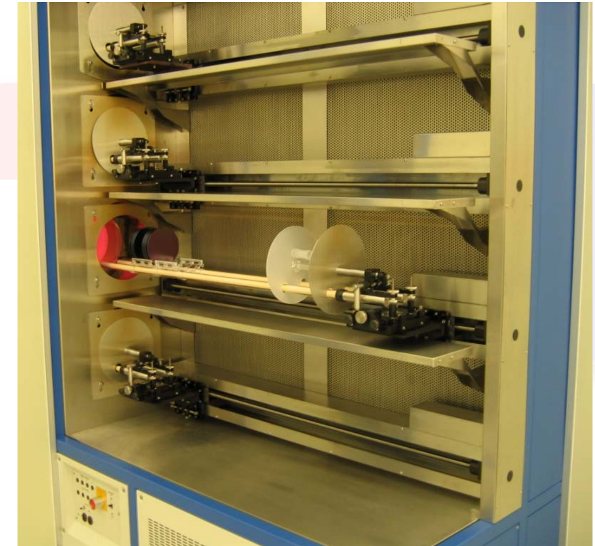
Gate

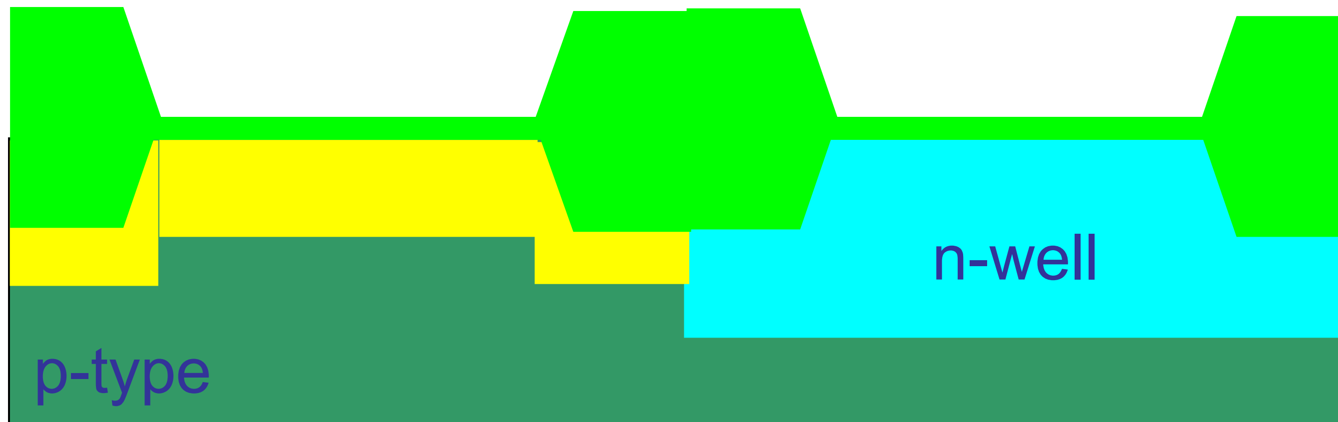
Resist strip



Gate

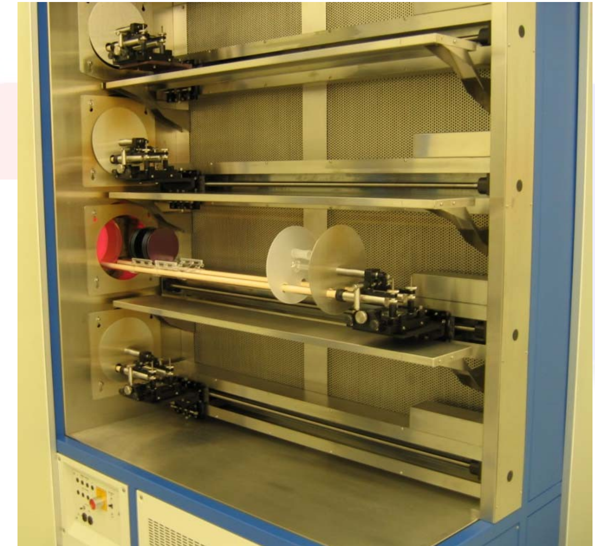
Anneal : N





Gate

Etch WR oxide + Gate oxidation (25 nm)



Gate

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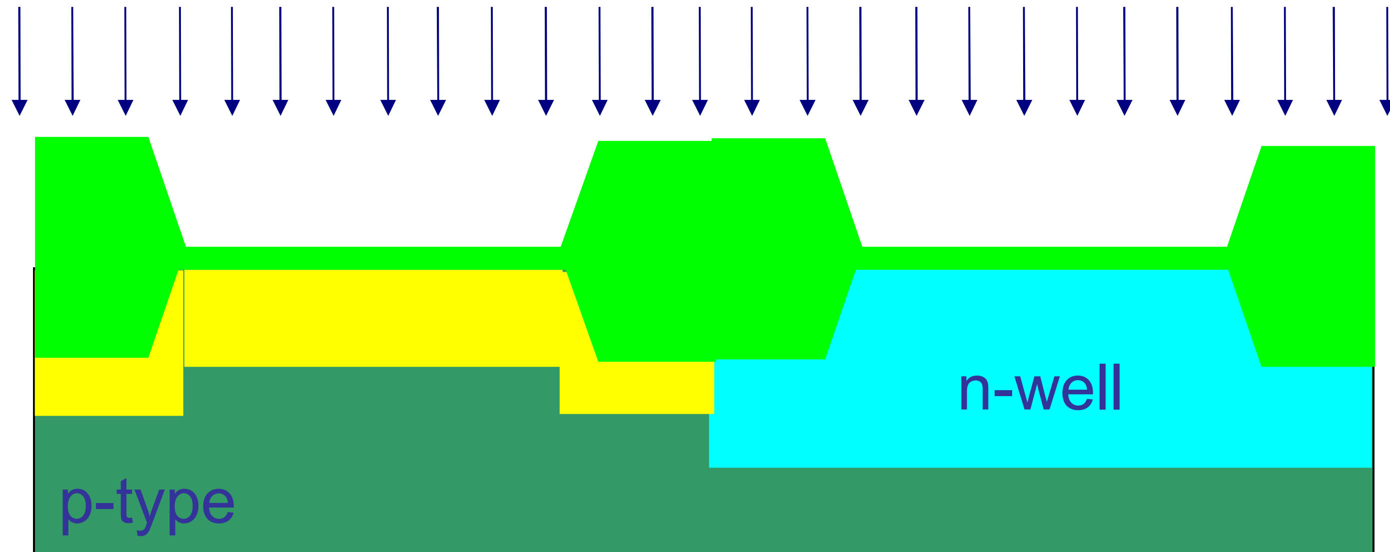
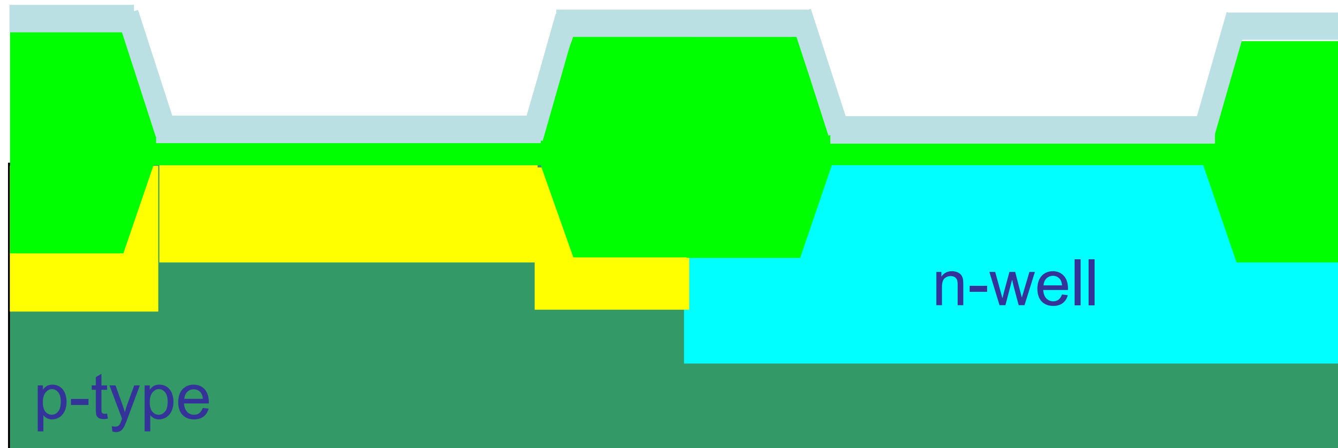
VTA implantation : Boron (8x10^{1} cm , 20 keV)



Gate

Poly deposition



Gate

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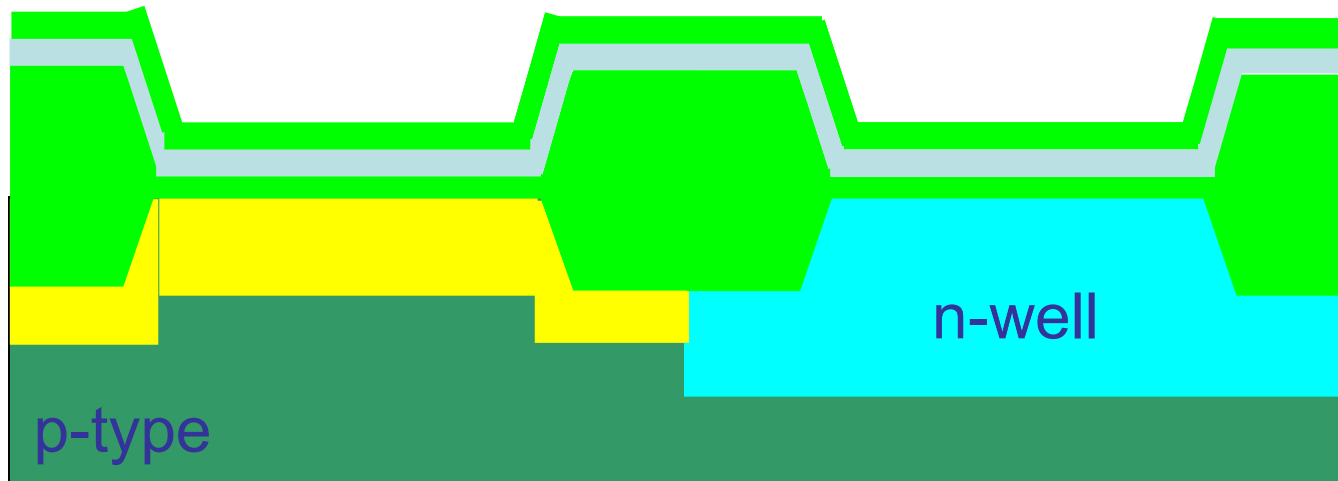
TEOS deposition



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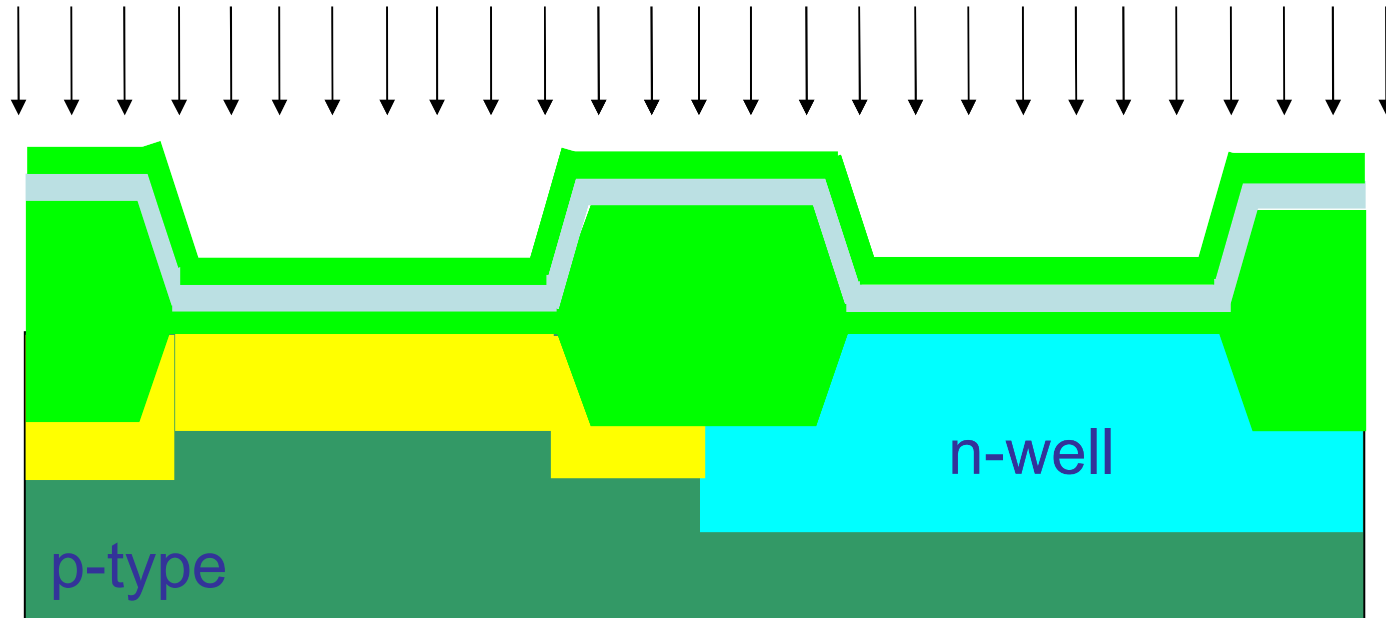
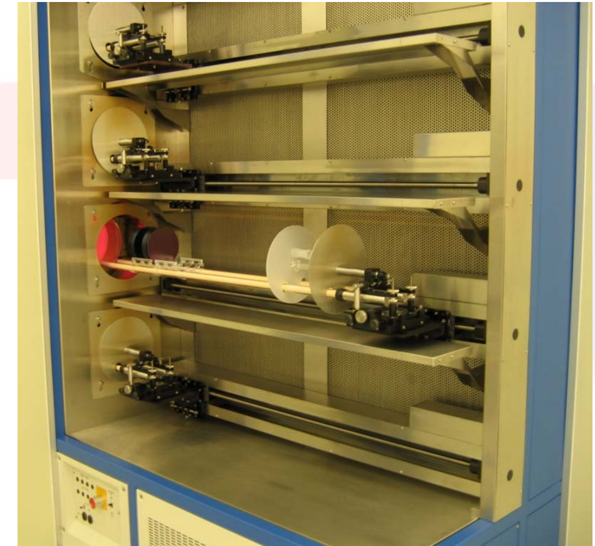
Gate

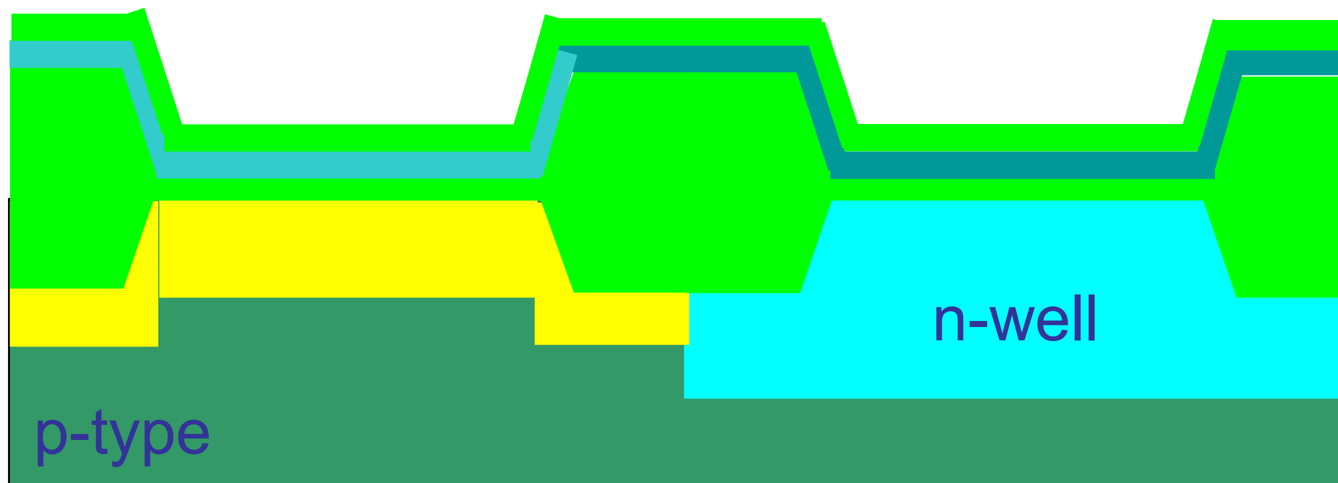
Poly implantation : Phosphorus
($1.2x10^{16}$ cm^{-3}, 50 keV)



Gate

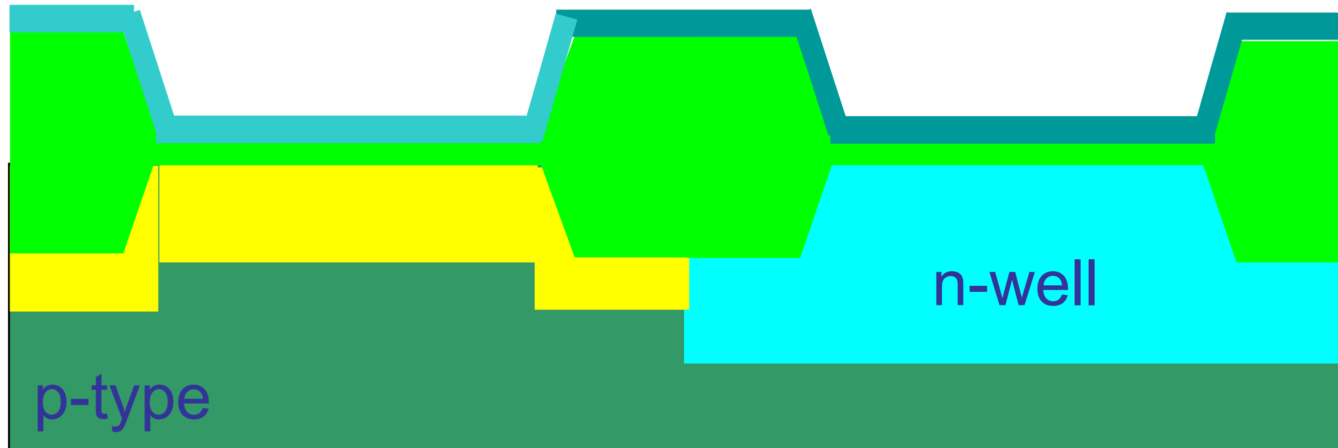
Anneal : N





Gate

Wet etch TEOS



Gate

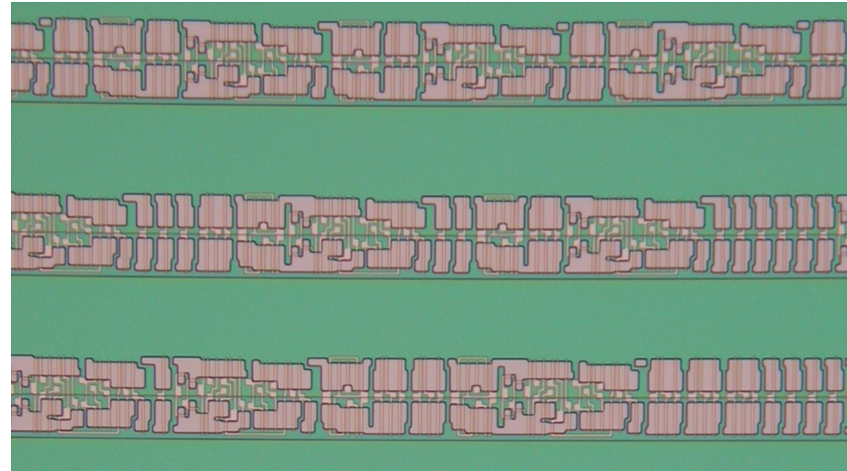
Photolithography : POLY

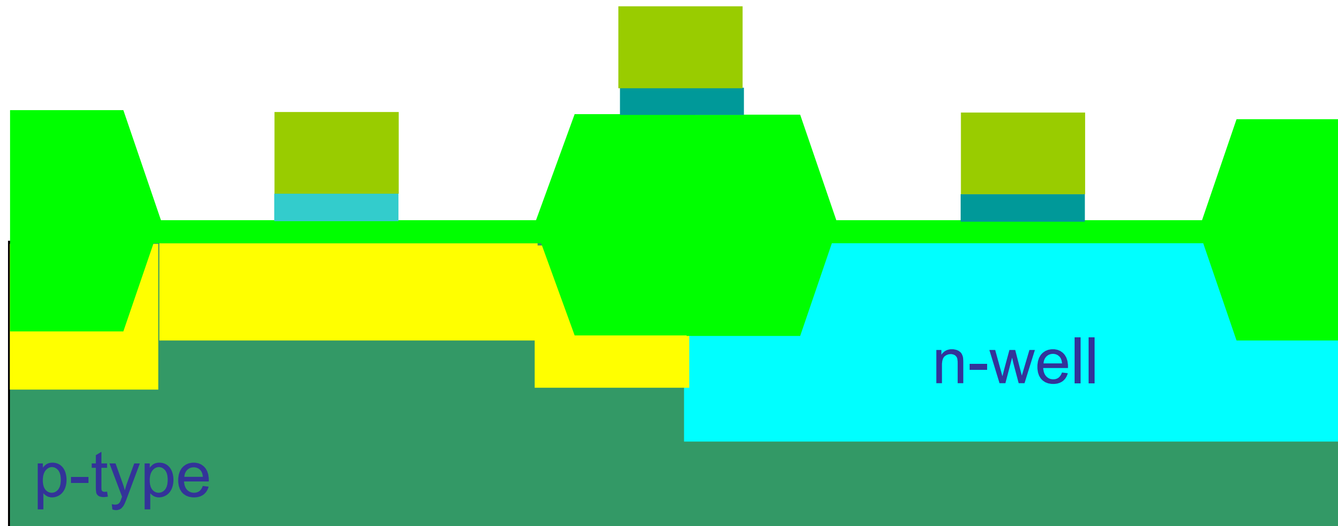
n-well

p-type

Gate

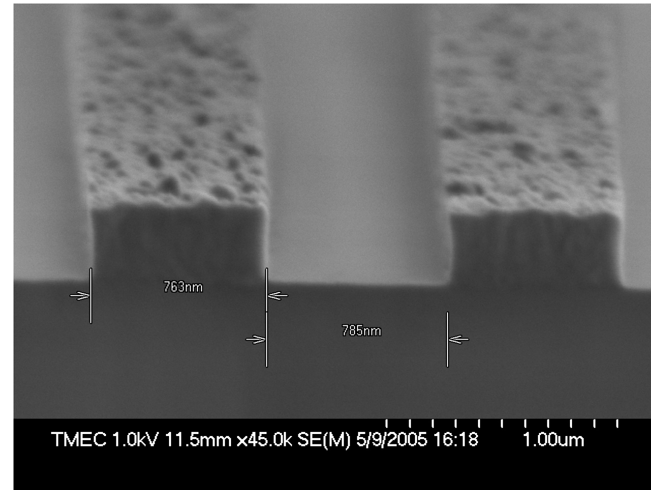
Dry etch poly

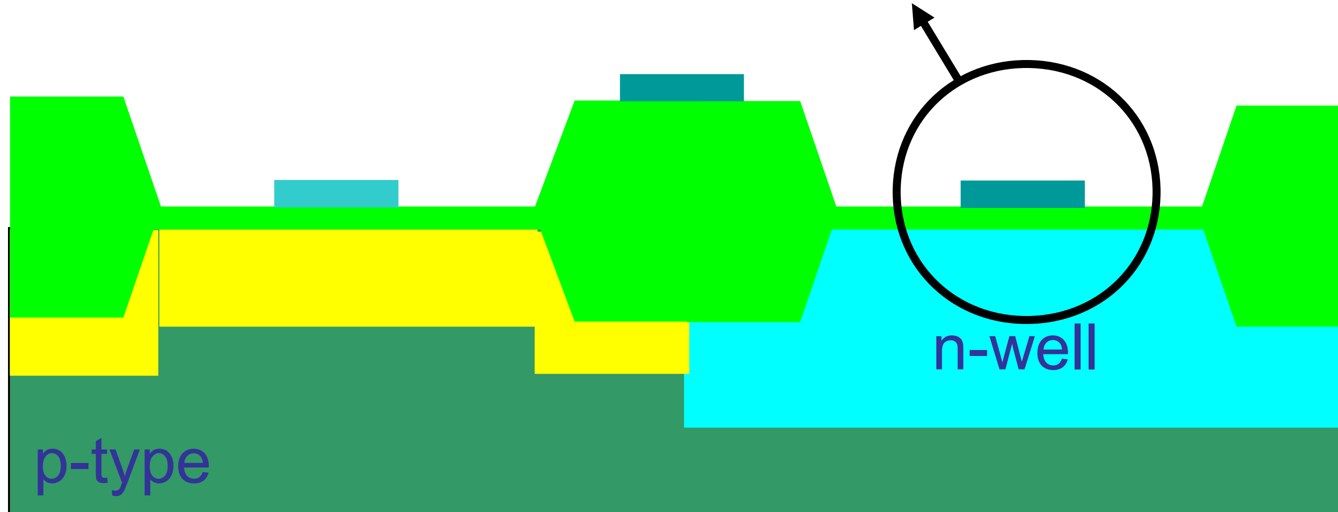




Gate

Resist strip





Process flow

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p-type Silicon Substrate

1. Starting wafer
2. n-well
3. Active
4. Gate
5. Junction
6. ILD
7. Contacts and metal 1
8. Vias and metal 2
9. Passivation

Junctions

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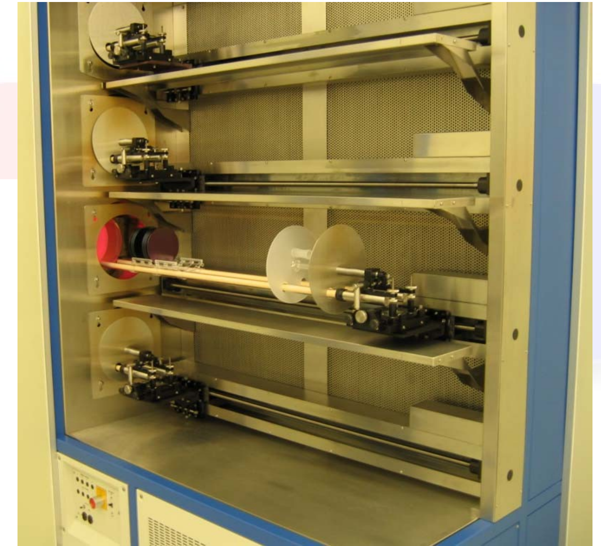
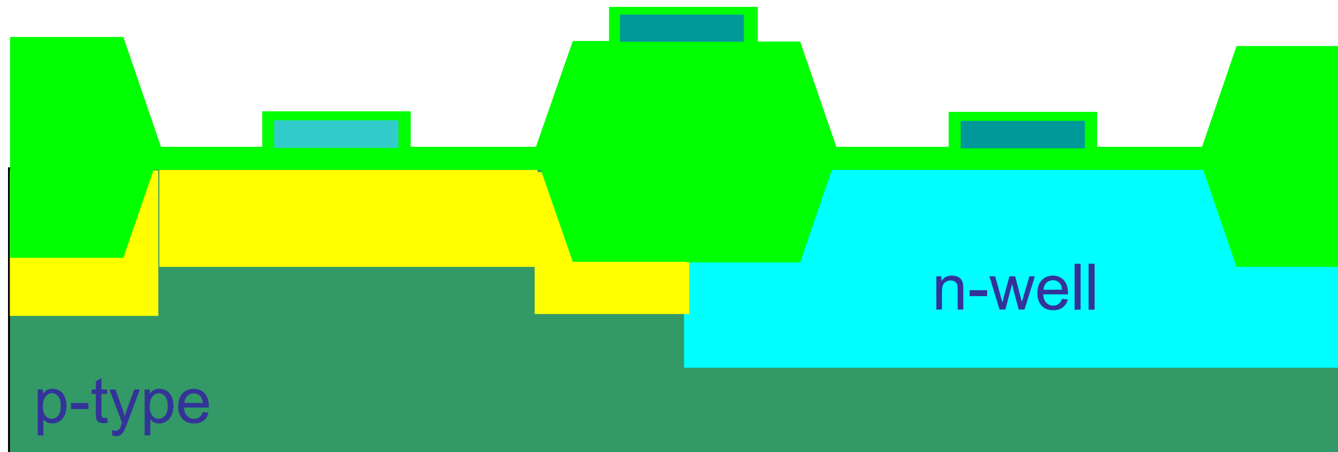
Oxidation : O





Junctions

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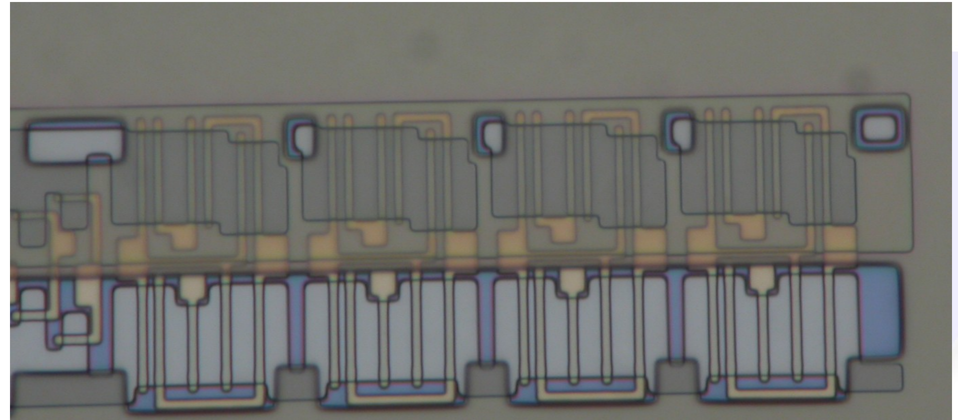
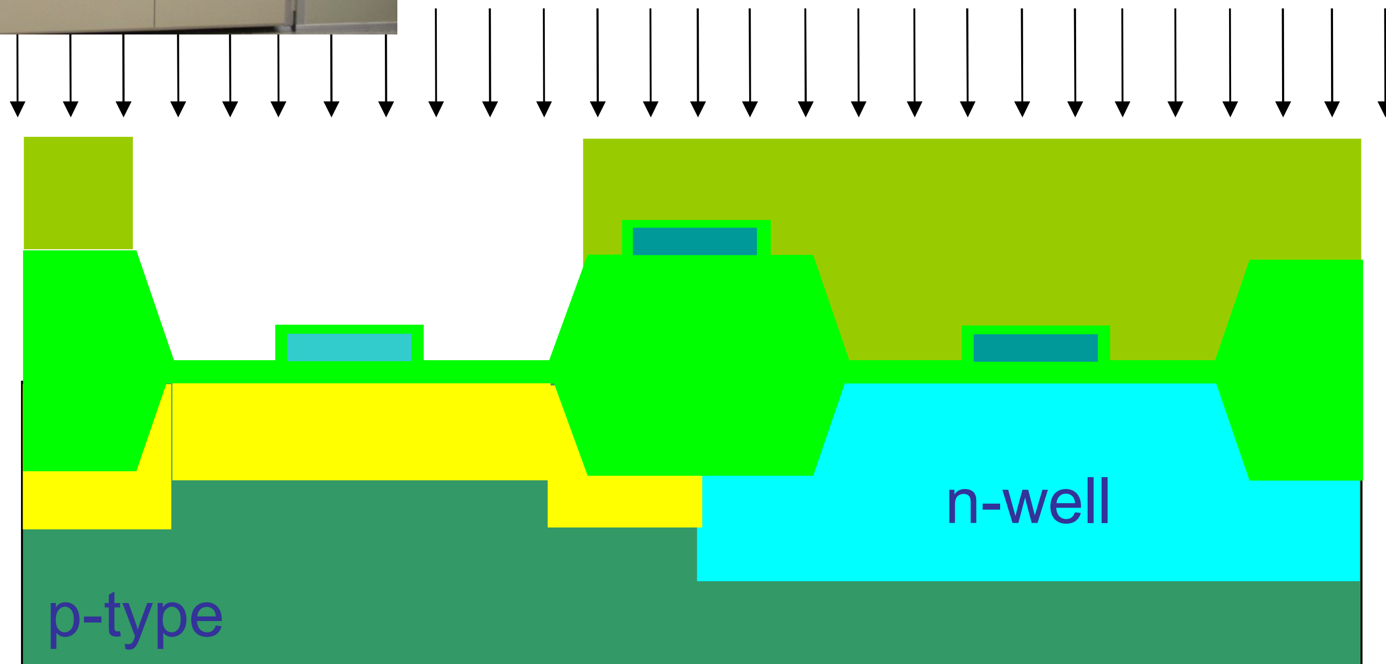
Photolithography : NPLUS



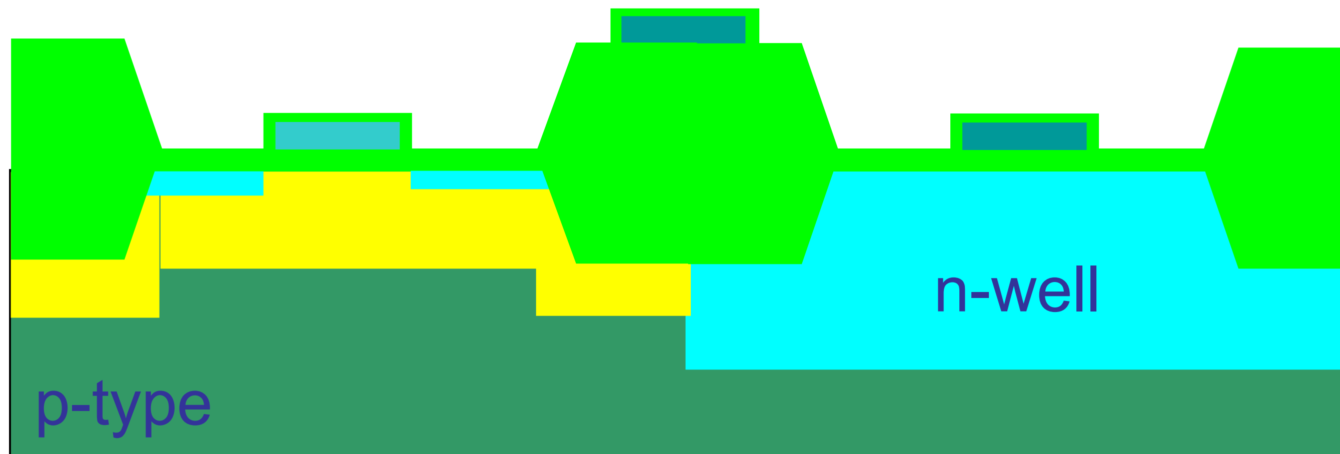
Junctions

Nplus implantation :
Phosphorus (10 cm , 70 keV)
Arsenic (6x10 cm , 130 keV)



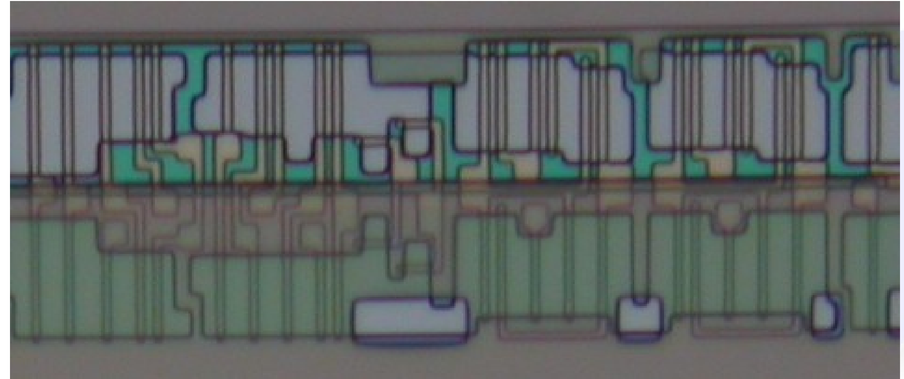
Junctions

Resist strip



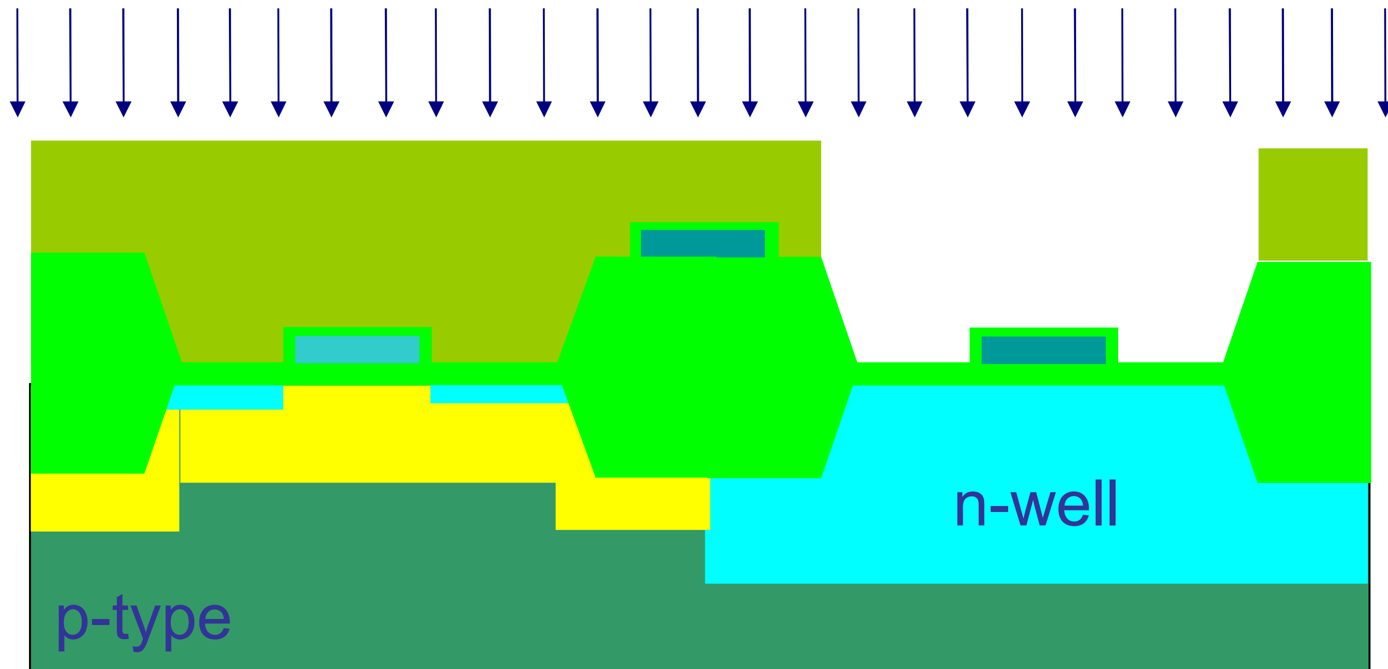
Junctions

Photolithography : PPLUS



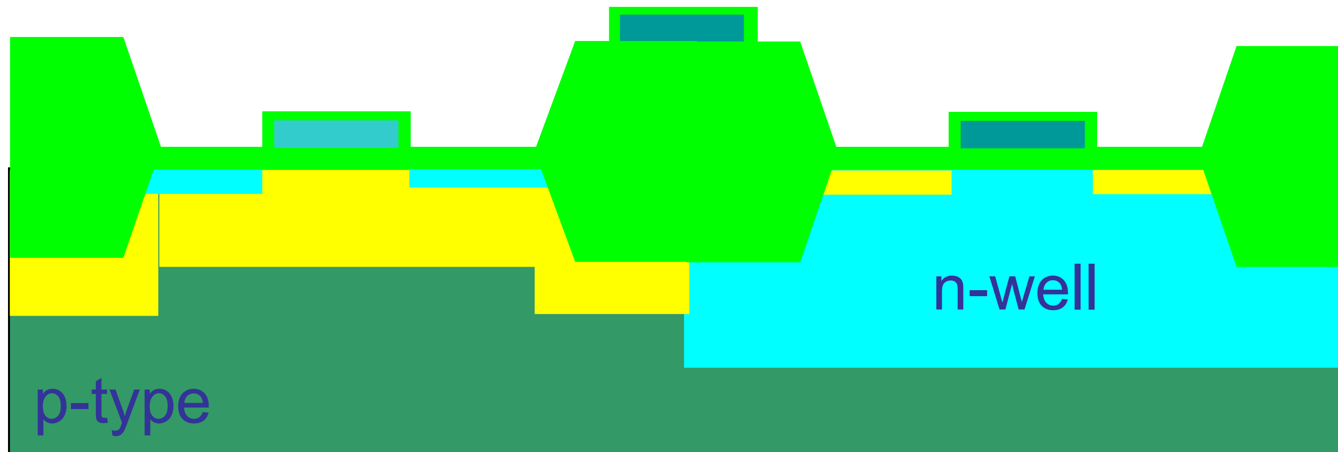
Junctions

Pplus implantation :
Boron ($5x10^{15}$ cm^{-2}, 20 keV)



Junctions

Resist strip



Junctions

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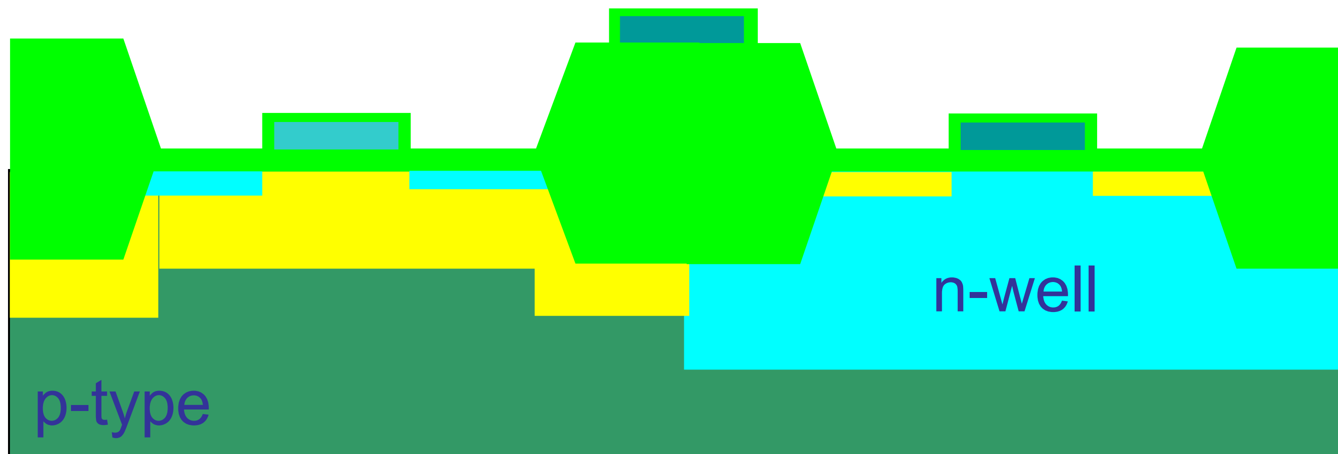
Coat front + Backside etch

Junctions

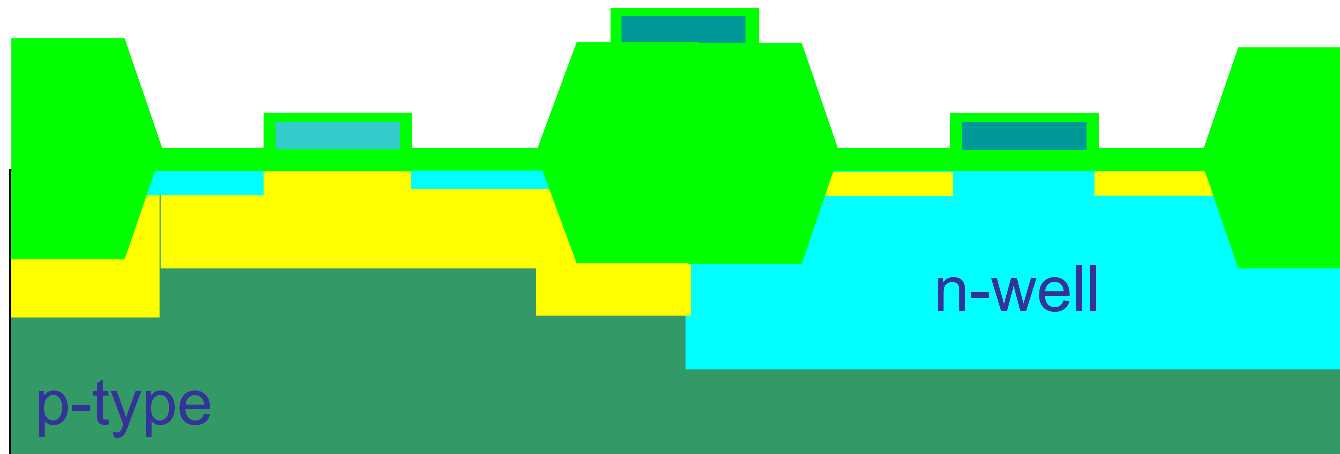
Resist strip



Junctions

Thai Microelectronics Center

Rapid thermal anneal : N



Process flow

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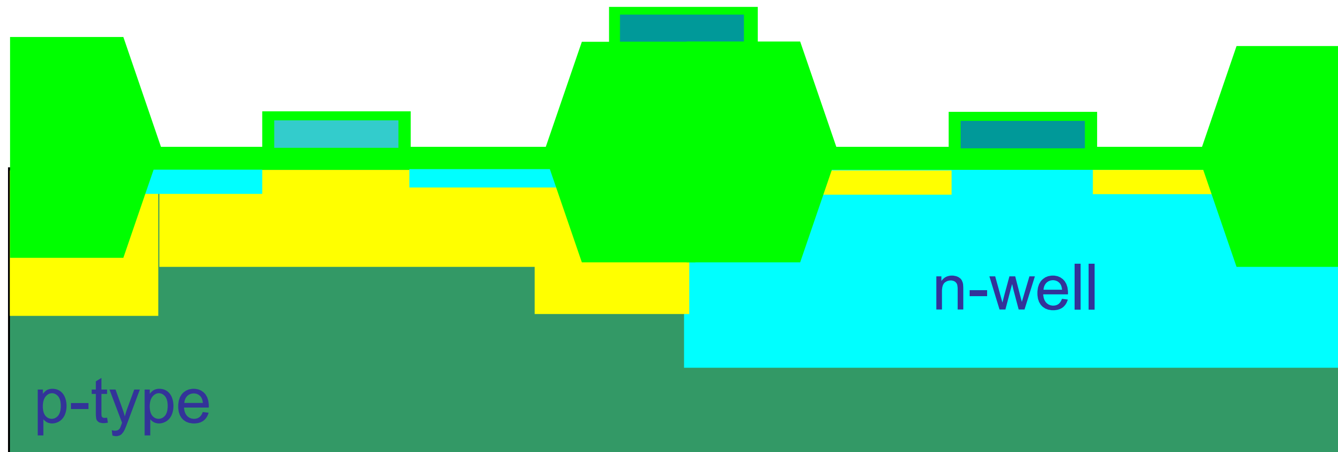
p-type Silicon Substrate

1. Starting wafer
2. n-well
3. Active
4. Gate
5. Junction
6. Interlayer Dielectric (ILD)
7. Contacts and metal 1
8. Vias and metal 2
9. Passivation

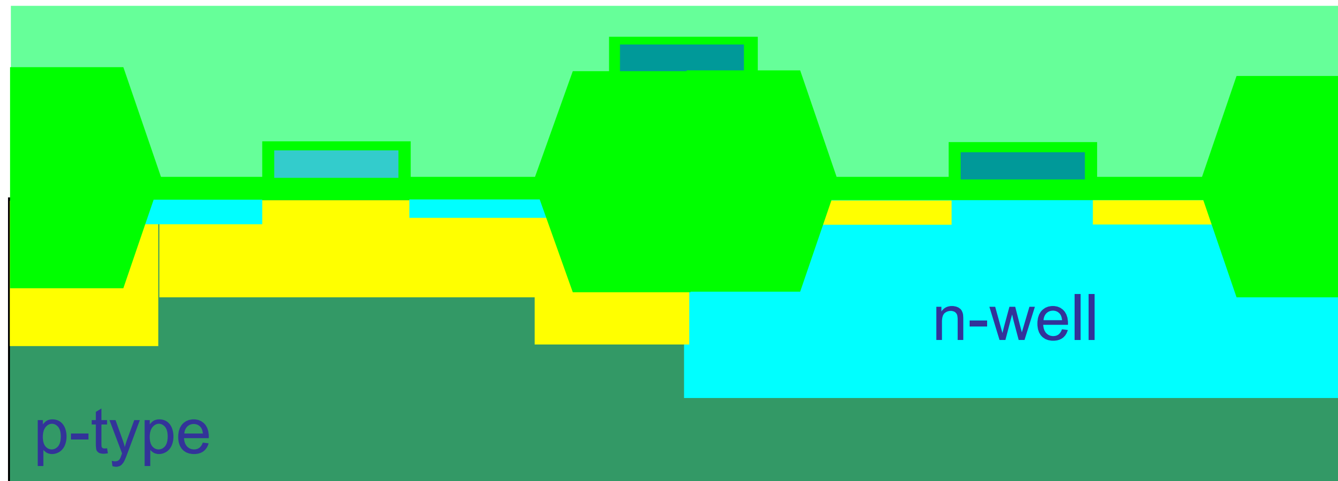
Interlayer Dielectric

TEOS deposition : UTEOS



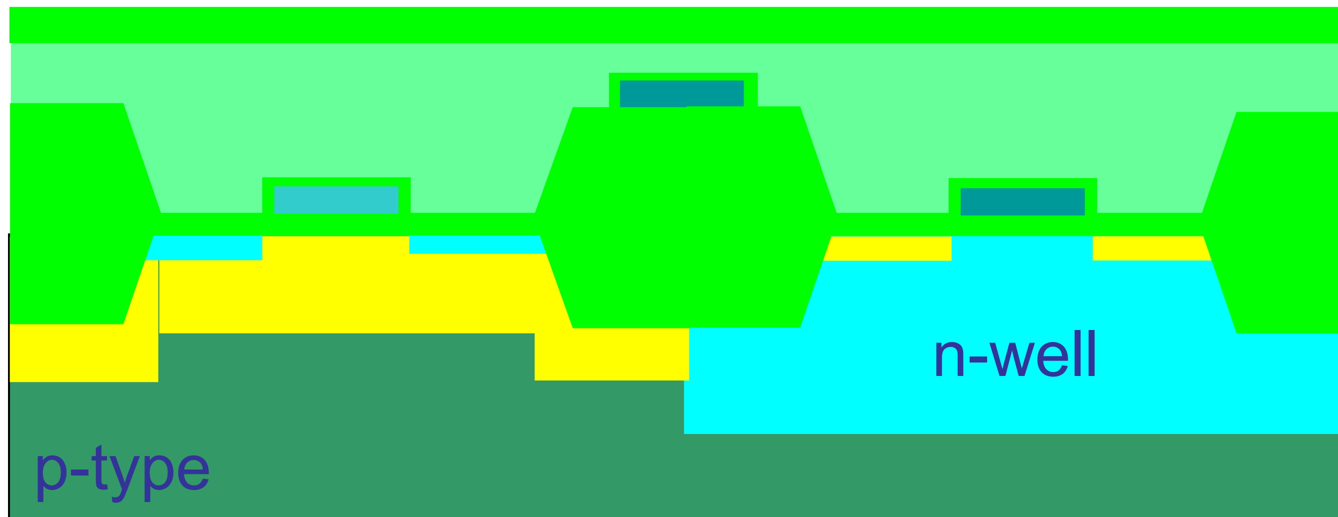
Interlayer Dielectric

SOG coat
SOG cure
SOG coat
SOG Cure



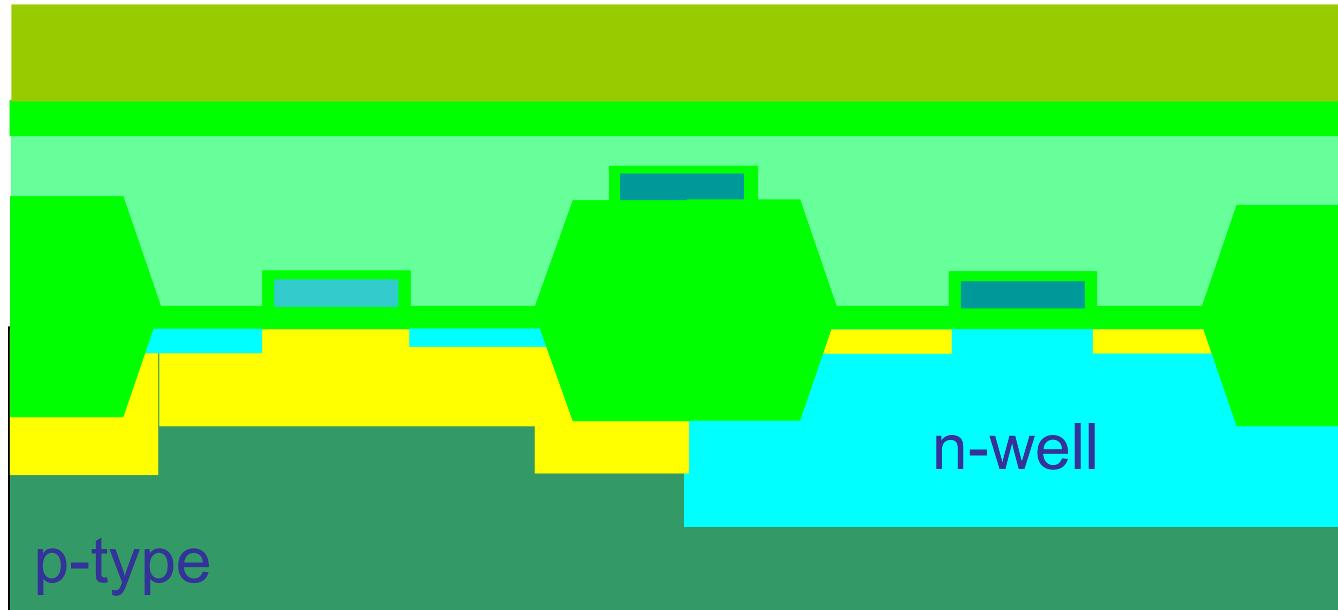
Interlayer Dielectric

PSG deposition
PSG densification



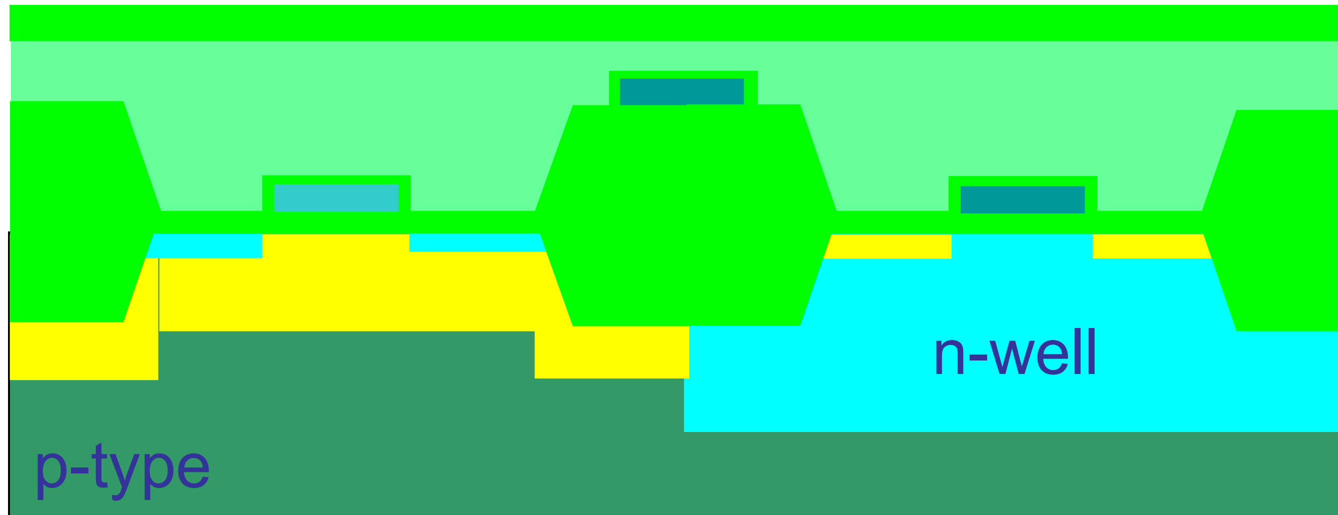
Interlayer Dielectric

Coat front
Backside etch



Interlayer Dielectric

Resist strip



Process flow

TMEC
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p-type Silicon Substrate

1. Starting wafer
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6. ILD
7. Contacts and metal 1
8. Vias and metal 2
9. Passivation

Contacts and Metal1

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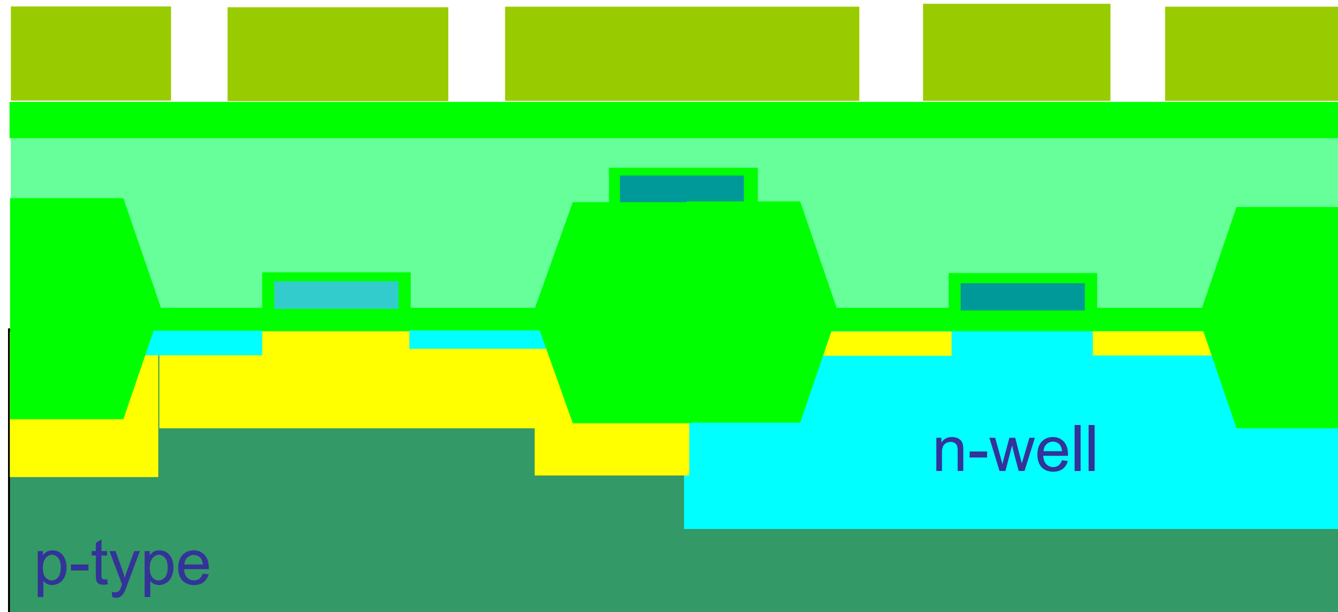
Photolithography : CONTACT



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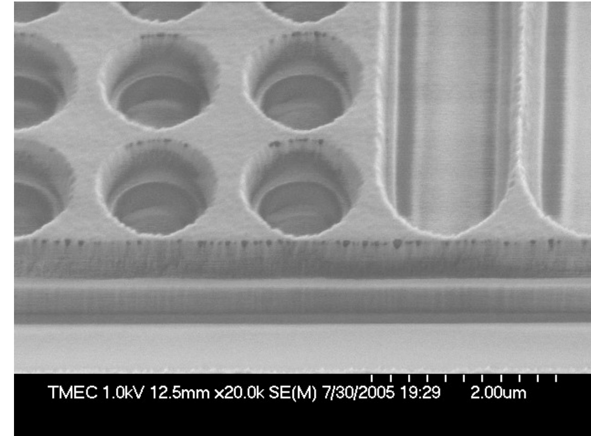
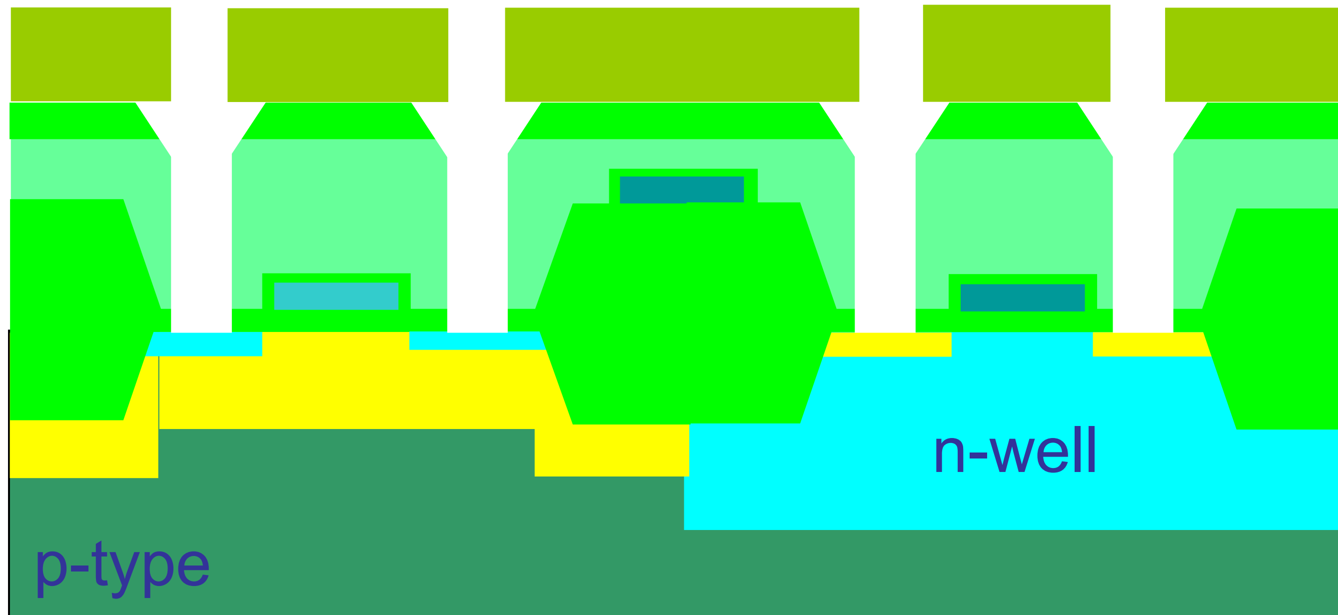
Contacts and Metal1

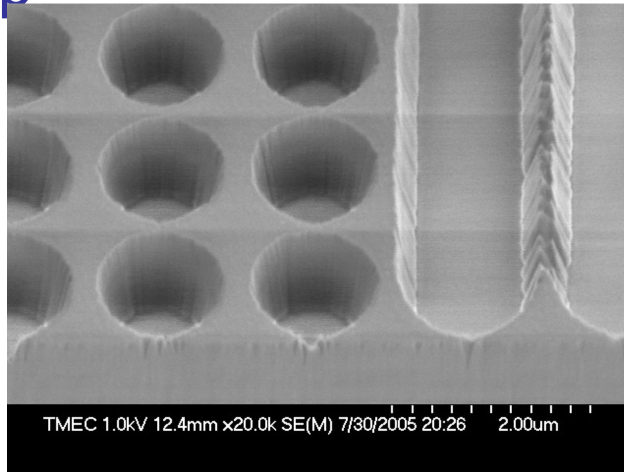
Dry etch contacts :
isotropic + anisotropic

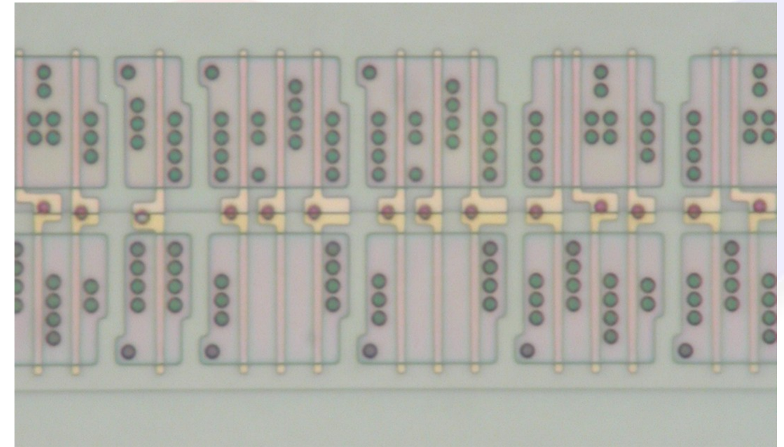


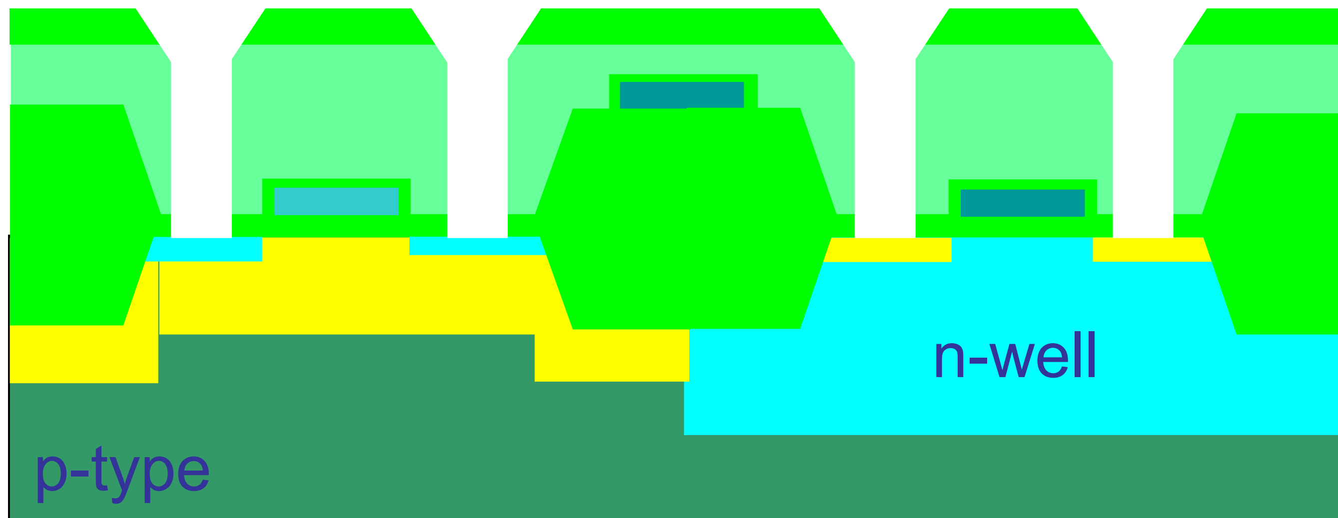


Contacts and Metal1

Resist strip



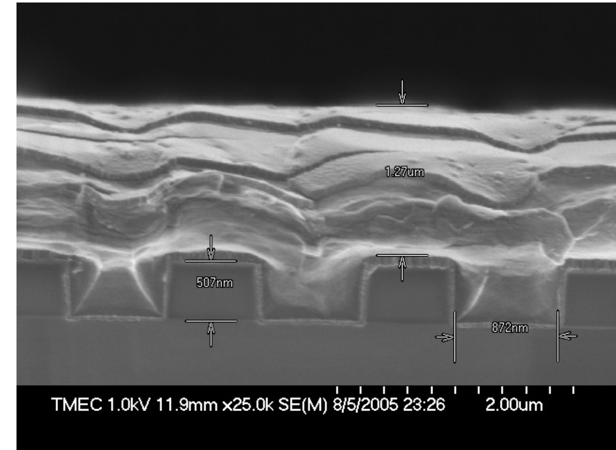


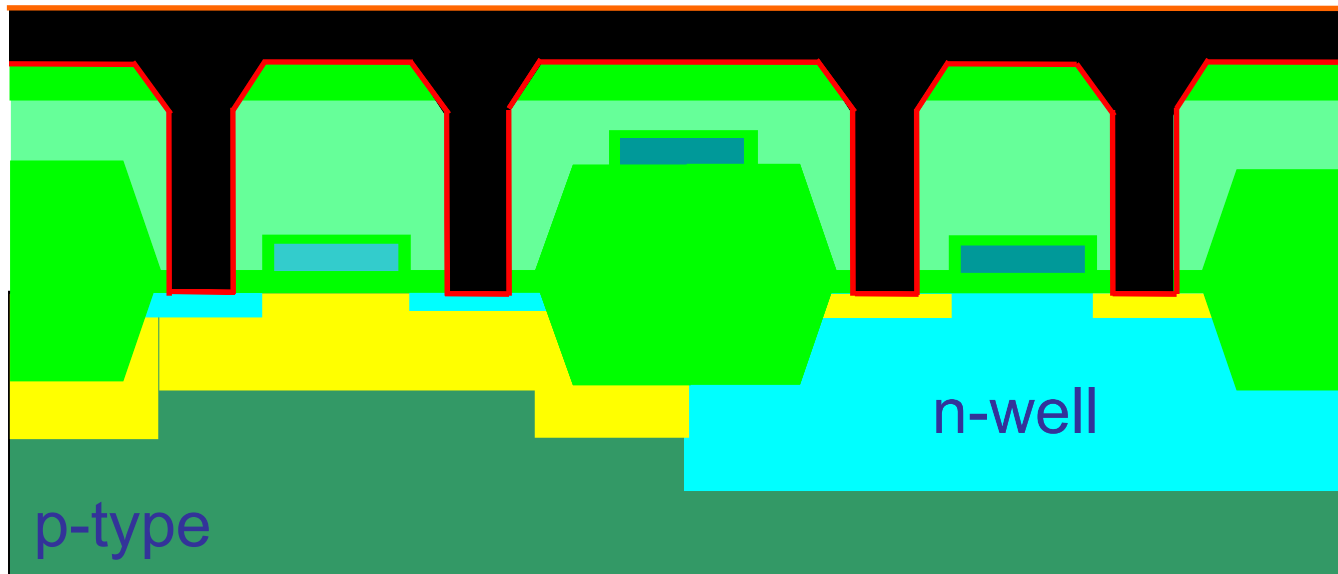


Contacts and Metal1

TMEC
Thai Microelectronics Center

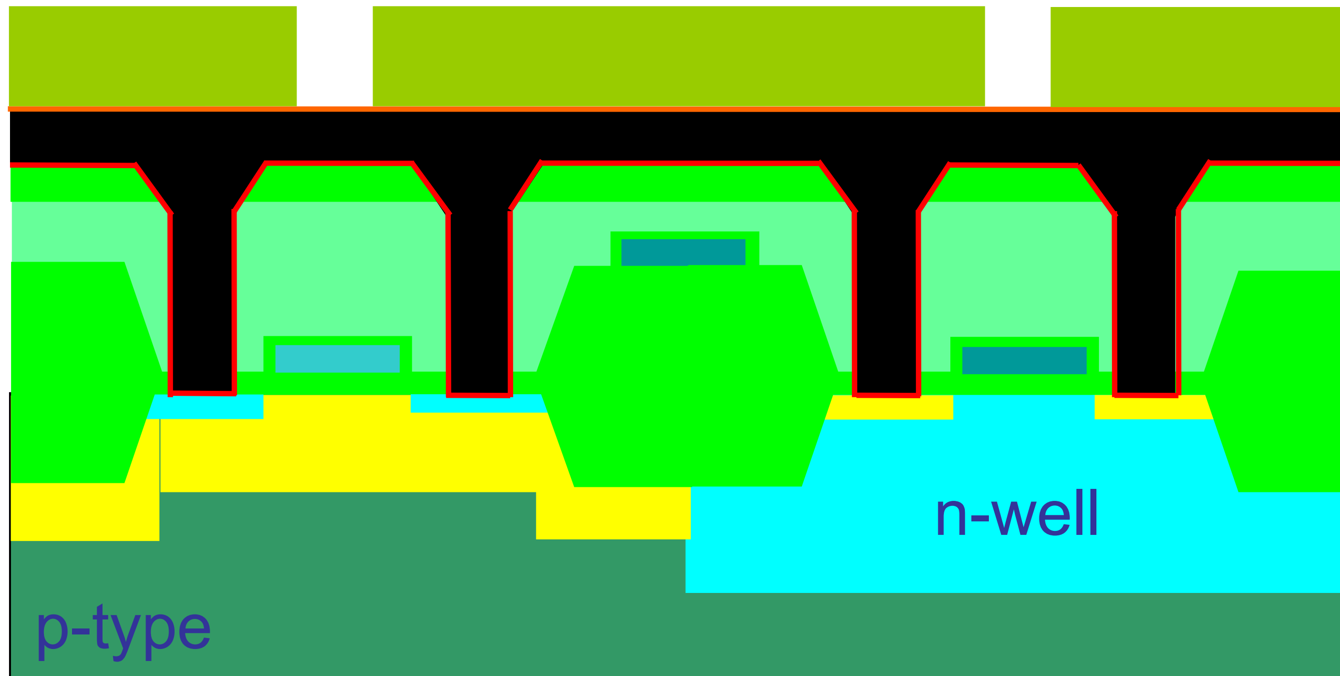
Contract clean
Metal 1 sputtering : TiTiN
AlSiCu
TiN





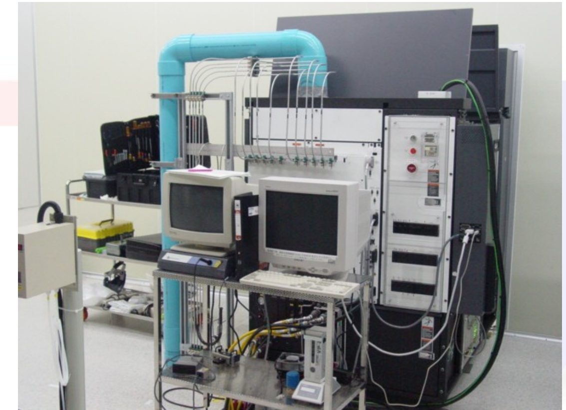
Contacts and Metal1

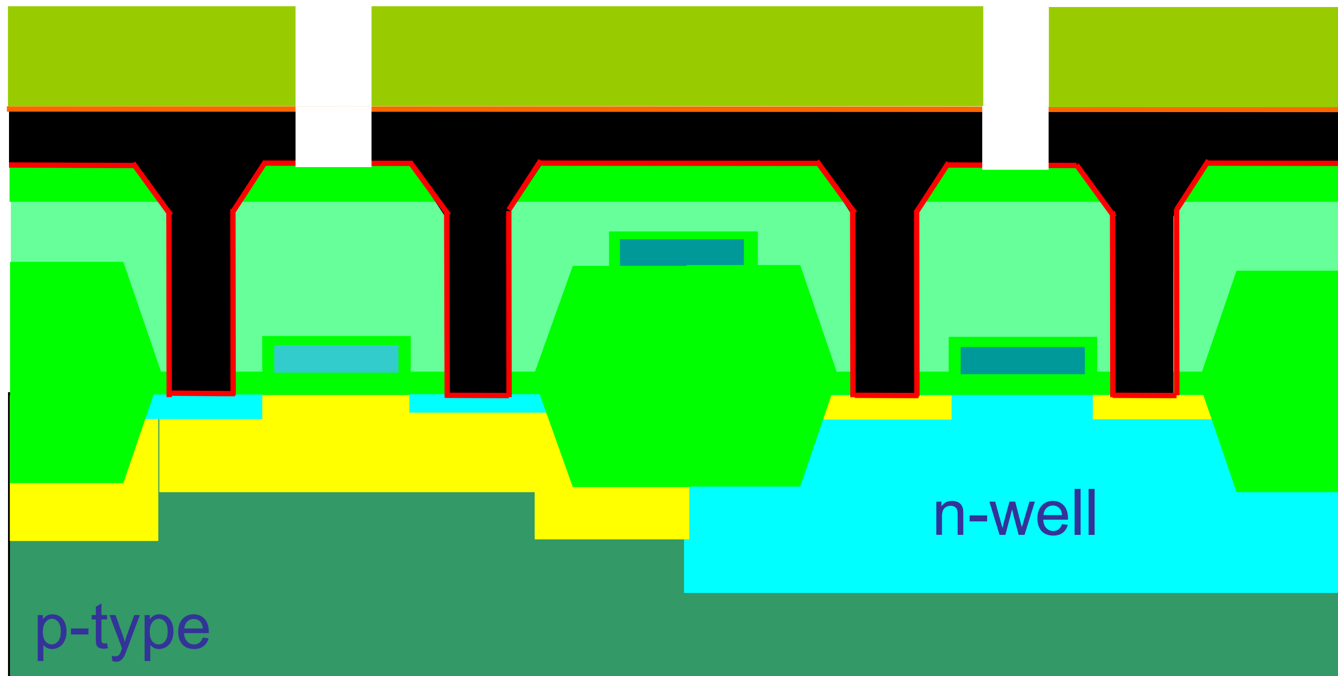
Photolithography : METAL1



Contacts and Metal1

Dry etch Metal 1

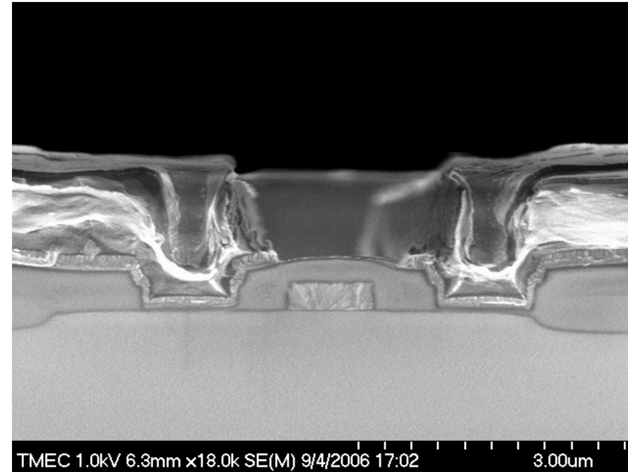


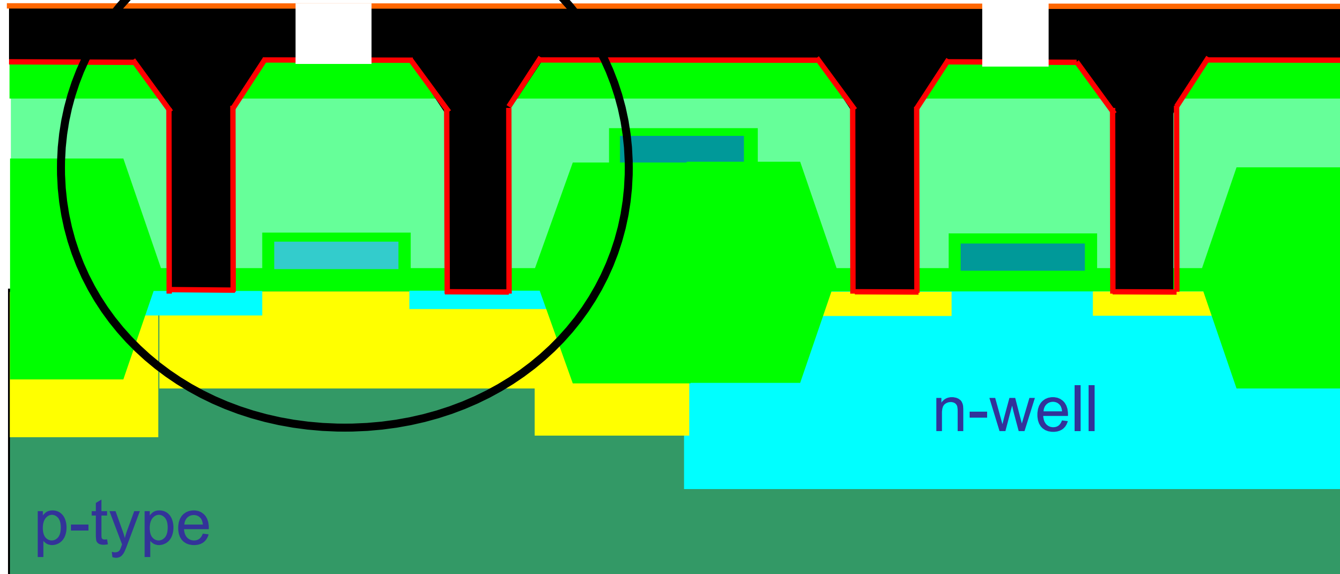


Contacts and Metal1

TMEC Thai Microelectronics Center

Resist strip





Process flow

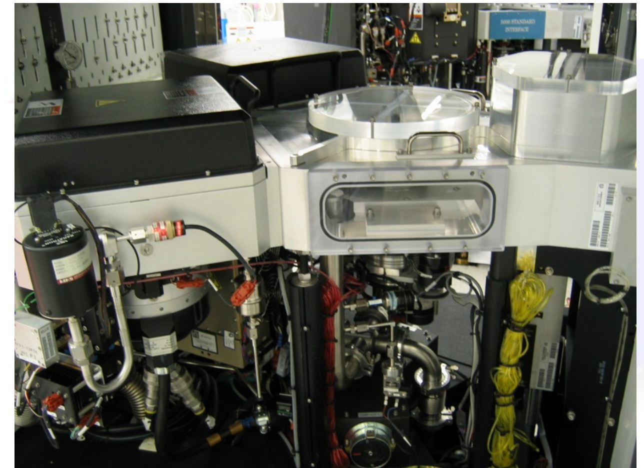
TMEC
Thai Microelectronics Center

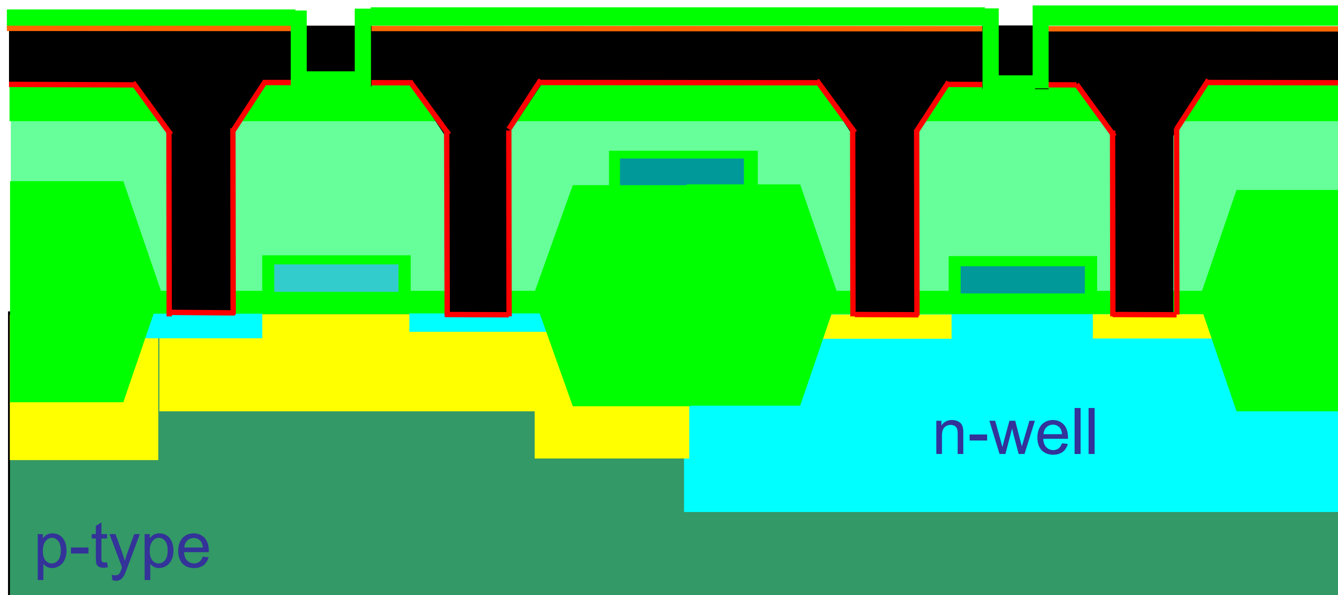
p-type Silicon Substrate

1. Starting wafer
2. n-well
3. Active
4. Gate
5. Junction
6. ILD
7. Contacts and metal 1
8. Vias and metal 2
9. Passivation

Via and Metal2

Plasma oxide deposition





Via and Metal2

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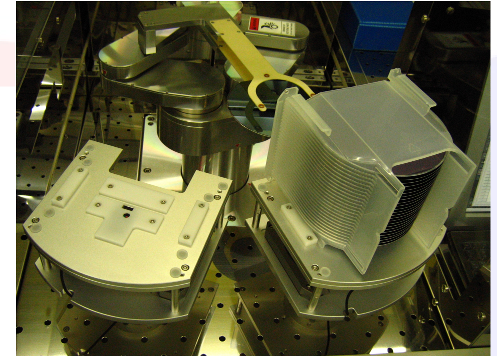
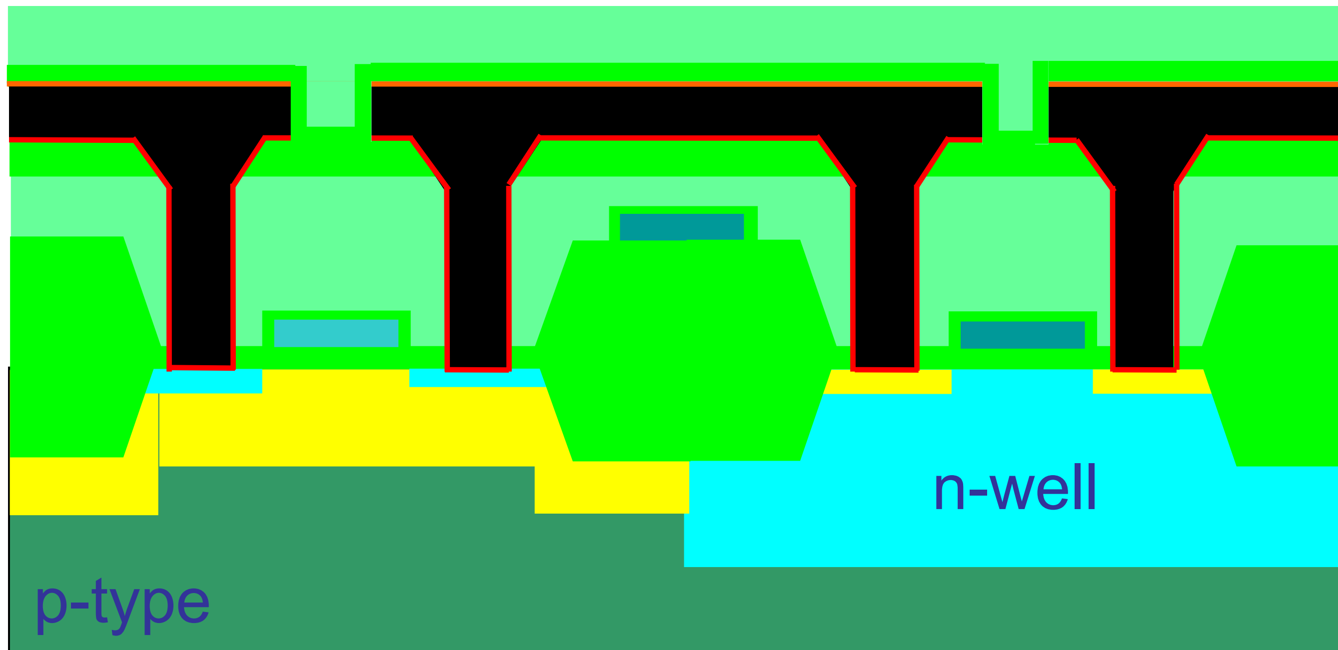
Thai Microelectronics Center

SOG coat
SOG cure

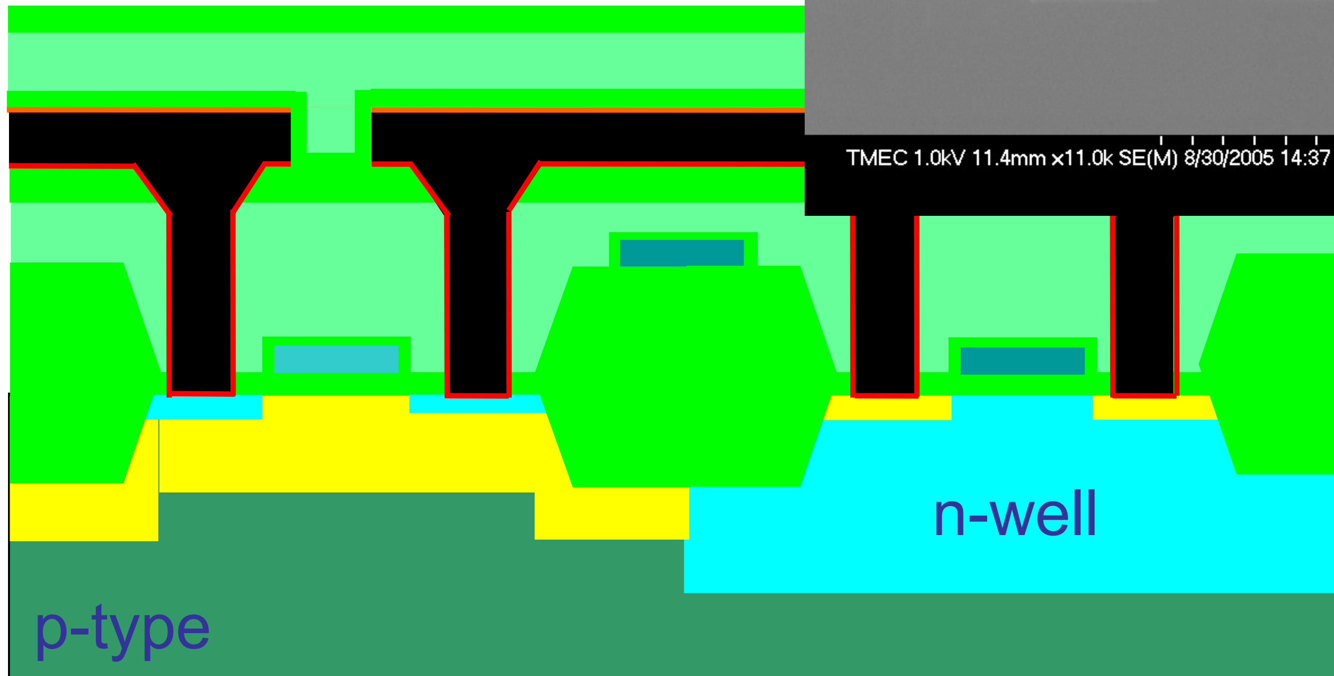


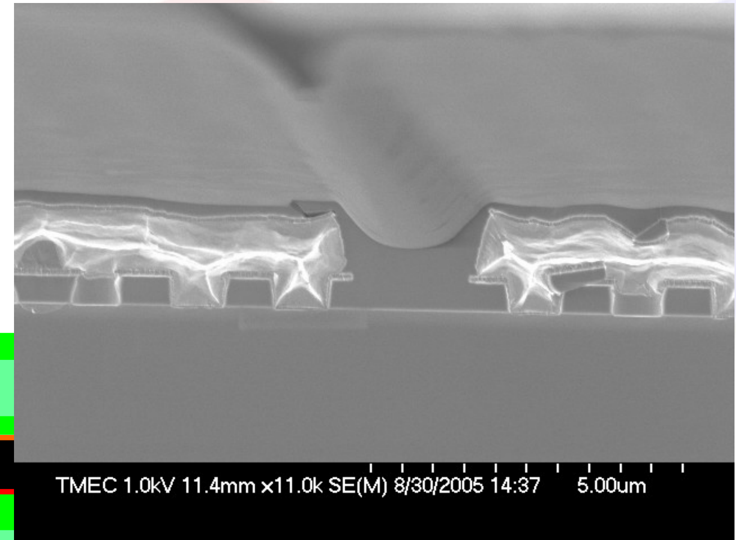


สวทช NSTDA
NECTEC
a member of NSTDA

Via and Metal2

Plasma oxide deposition





Via and Metal2

Photolithography : VIA

n-well

p-type

Via and Metal2

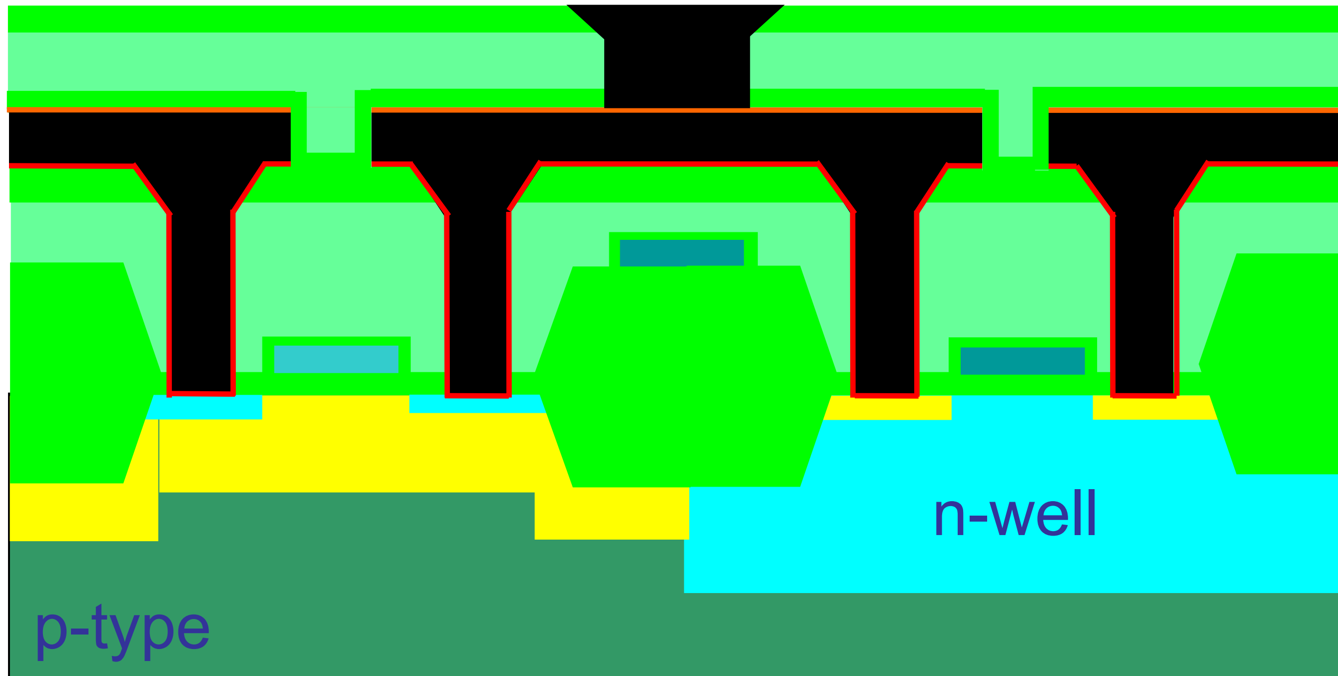
Dry etch vias : isotropic + anisotropic

n-well

p-type

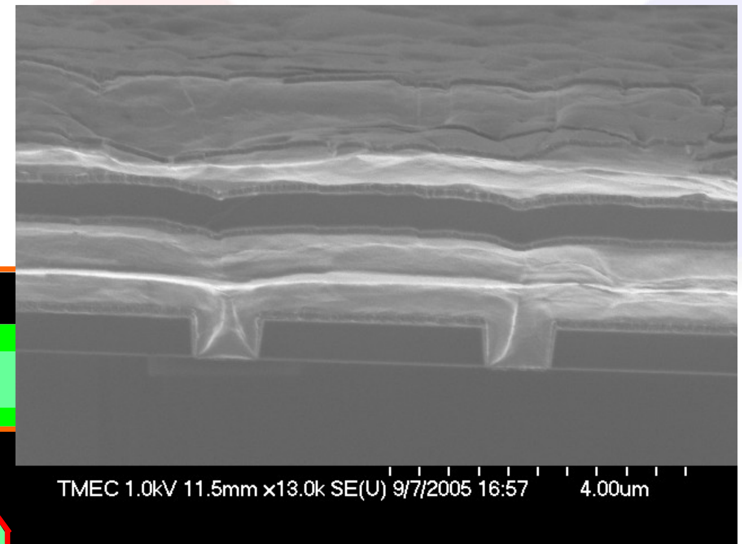
Via and Metal2

Resist strip



Via and Metal2

Metal2 sputtering : AlsiCu
TiN



n-well

p-type

Via and Metal2

Photolithography : METAL2

n-well

p-type

Via and Metal2

TMEC
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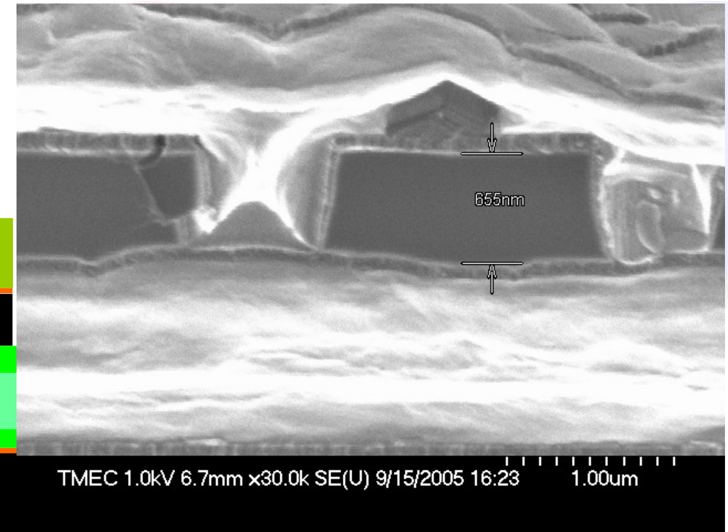
Dry etch metal2



n-well

p-type

Via and Metal2

Resist strip

n-well

p-type

Process flow

TMEC
Thai Microelectronics Center

p-type Silicon Substrate

1. Starting wafer
2. n-well
3. Active
4. Gate
5. Junction
6. ILD
7. Contacts and metal 1
8. Vias and metal 2
9. Passivation

Passivation

PECVD nitride deposition, Photolithography : PASS,
Dry etch nitride, Resist strip, Sintering : Forming gas