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Extraction of Defect in Doping Silicon Wafer by Analyzing the Lifetime Profile Method

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Abstract. The total leakage current in silicon p-n junction diodes compatible with 0.8 μm CMOS technology is investigated. The generation lifetime is a key parameter for the leakage current, which can be obtained from the current-voltage (I-V) and the capacitance-voltage (C-V) characteristics. As will be shown, the electrically active defect from ion implantation process generated in p-n junction can be extracted from the generation current density.

Introduction

The development of modern complementary metal-oxide- semiconductor (CMOS) technology is aiming to increase performance per chip and reduce cost [1]. This technology is not only use to produce microchip and can also be applied to fabricate smart sensor. This helps to integrate several kind of sensors together. For reasonable cost to produce these devices, 0.8μm CMOS technology is usable. In this technology a high substrate doping concentration is required in order to control the short-channel effects and lowering leakage current. The p-well or n-well concentration is increased by an increasing ion implantation dose. This process introduces a substrate damage, which is expected to be removed after annealing [2]. A low temperature and short time thermal treatment is needed to maintain the junction depth after ion implantation, which may not sufficient to remove the implantation-induced defects [3]. These defects can be a source of the leakage current in each of p-n junction. The leakage current in p-n junction is one of the main parameters that affect device performance. This leakage current is related to electrically active defects in the silicon. The defects determine generation (τ_g) lifetime. Therefore, one way to study defects is by analyzing the lifetime. Usually, it can be extracted from the generation current [4].

Experimental

For this study, shallow p-n junction diodes compatible with 0.8 micron CMOS technology was fabricated on 150 mm 5 Ω-cm p-type silicon substrate. The n-well was obtained by 140 keV, $4x10^{12}$ ions/cm^2 phosphorus implantation. The n^+ region was made by 50 keV, $5x10^{15}$ ions/cm^2 arsenic implantation and 40 keV, $3x10^{15}$ ions/cm^2 boron implantation for the p^+ region. Finally, the junction was contacted by aluminum metallization. In order to study the leakage current components, a difference area (A) and perimeter (P) diodes have been fabricated on wafer. Square (SQ) diode has A=$8x10^{-4}$ cm^2 and P= 0.12cm, while Meander (ME) diode has A=$8x10^{-4}$ cm^2 and P= 8.04cm. The current-voltage (I-V) characteristics of the different geometry diodes were measured on wafer with bias step of 0.01 V. from reverse (V_R) to forward (V_F)voltage, in range of –5 to +1 V, whereby the bias was applied to the back p-type substrate (or n_{well}) and the current was measured at the top n-type (or p^+). The temperature (T) was controlled at 25 ^oC, in dark shield box. The capacitance-

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voltage (C-V) characteristics were performed on the same diode with the frequency of 1 MHz at 25 ^{o}C. The area depletion width in the substrate can be extract from C-V characteristics.

Results and Discussion

The analysis strategy can be summarized as follows. The total reverse current (I_R) of p-n junction consists of different geometrical components, the area leakage current (I_A) and the peripheral leakage current (I_P) and given by [5]

$$I_R = AJ_A + PJ_P \tag{1}$$

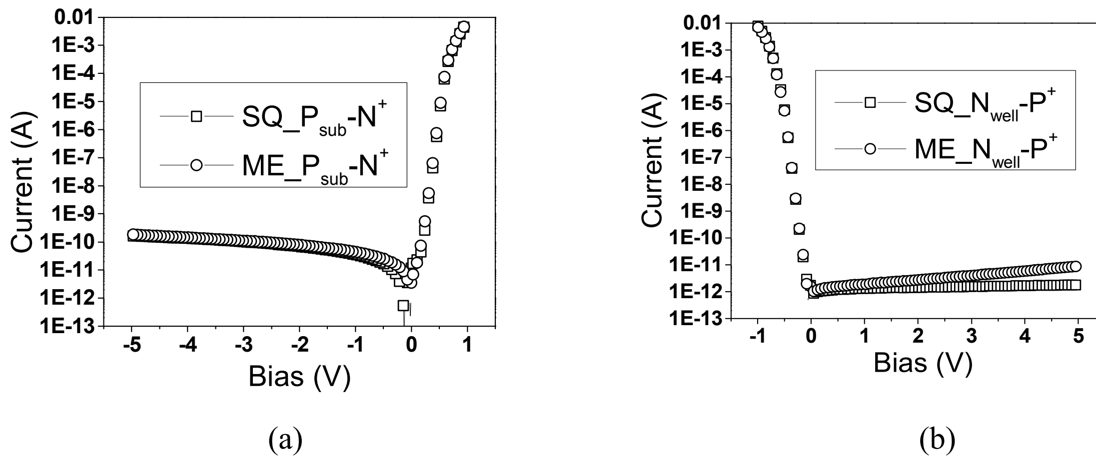
$$J_A = \frac{qn_iW_A}{\tau_g} + J_{Ad} \tag{2}$$

For $J_{Ad} << J_A$, τ_g can be calculated from

$$\tau_g = \frac{qn_iW_A}{J_A} \tag{3}$$

where J_A (A/cm^2) is the area current density scaling with the diode area (A), J_P (A/cm) is the perimeter current density scaling with the perimeter (P). J_{Ad} is area diffusion current density, q (C) is electron charge (=1.602x10^{-19} C), n_i (cm^{-3}) is intrinsic carrier concentration (=1.08x10^{10} cm^{-3}), W_A (cm) is area depletion width and τ_g (s) is generation lifetime.

Figure 1 shows a plot of current versus voltage. By combining difference geometry diodes and using Eq.1, the area and perimeter leakage current can be extracted from the leakage current (Fig. 1), as shown in Fig. 2.



(a) (b)

Figure 1. The current-voltage characteristics for the different diodes (a) n^{+} - P_{sub} junction diode and (b) p^{+} - N_{well} junction diode

As shown in Eq. 3, the generation lifetime depends on the area depletion width and the area current density. The area depletion width can be obtain from the area capacitance density (C_A)

$$W_A = \frac{\varepsilon_{si}\varepsilon_o}{C_A} \tag{4}$$

where ε_{si} is dielectric constant of silicon (=11.8) and ε_0 (F/cm) is permittivity of vacuum (=8.854x10^{-14} F/cm)

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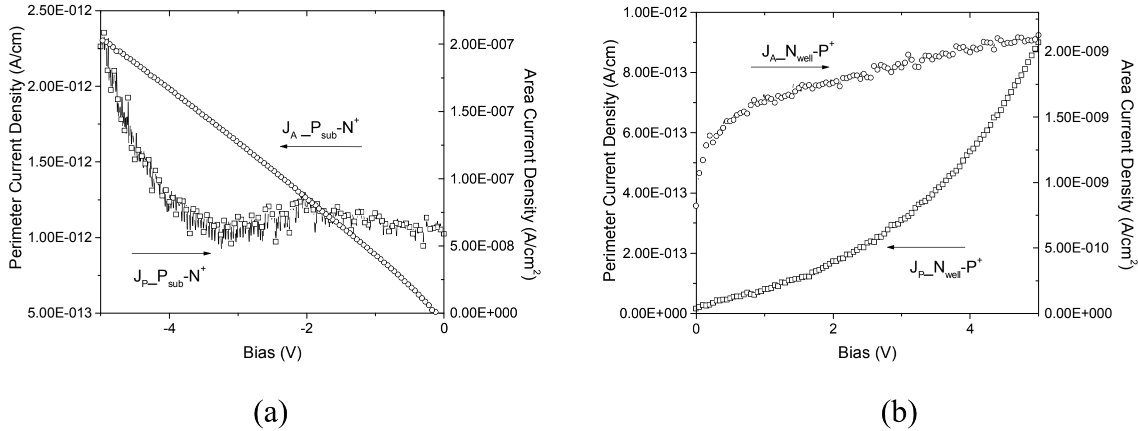


(a) (b)

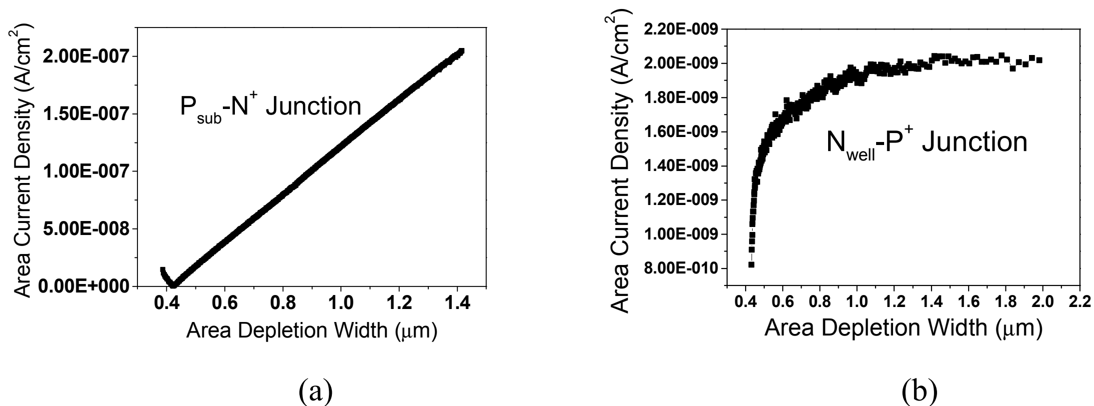
Figure 2. The current density for the different diodes (a) n^+ - P_{sub} junction diode and (b) p^+ - N_{well} junction diode

Similar to the current components and assuming that the total C_j is a linear combination of the different capacitance components, given by

$$C_j = AC_A + PC_P \tag{5}$$

where C_A (F/cm^2) is the area capacitance density, which scales with the diode area (A), C_P (F/cm) is the perimeter capacitance density, which scales with the diode perimeter (P)

Normally, the junction capacitance (Cj) is measured by monitoring the response of the junction to a small-signal voltage superimposed upon the dc voltage. The area capacitance density (C_A) and the perimeter capacitance density (C_P) can be assumed a linear combination of different geometrical components as given in Eq. 5. Area current density versus area depletion width for difference diodes are shown in Fig. 3. This figure indicates that the area depletion width increase with reverse bias. From the slope of the two curve is different, the n^+ - P_{sub} junction doping is uniform but the p^+ - N_{well} junction doping is gradient cause by the phosphorus implantation for N_{well} . Therefore, the increasing of the curve changes by the distribution of the phosphorus doping profile (lattice defect).



(a) (b)

Figure 3. The area current density versus area depletion width for the different diodes (a) n^+ - P_{sub} junction diode and (b) p^+ - N_{well} junction diode

The area current density can be calculated from Eq. 2. This shows that a linear relation between J_A and W_A will be obtained. The interception at $W_A = 0$ gives J_{Ad}, while the slope yield (qn_i / τ_g). From Fig. 3a indicates that τ_g is constant along W_A, which relates to the substrate doping uniformity. But, in case of Fig. 3b, τ_g is not constant due to n-well implantation induced defect.

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Finally, the generation lifetime (τ_g) can be obtained from Eq. 3. The plot of the generation lifetime versus the area depletion width are shown in Fig. 4. The Figure 4 shows that the generation lifetime of the n^+ - P_{sub} junction is less than the p^+ - N_{well} junction. This implies that the defect can be generated in the p^+ - N_{well} junction more than the n^+ - P_{sub} junction.

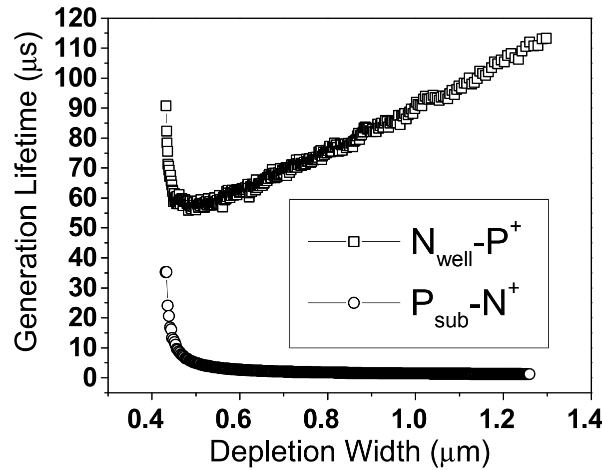

Figure 4. The generation lifetime versus the area depletion width of the different junction diodes.

Summary

The generation lifetime can be obtained from I-V and C-V characteristics of p-n junction. The implantation of phosphorus dopant can introduce defects. These defects cause a higher generation lifetime, which reduces generation current. This indicates that the junction leakage current can be reduced by introduction higher generation lifetime defects.

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